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# AUTOMATED ARRAY ASSEMBLY TASK

# IN-DEPTH STUDY OF SILICON WAFER SURFACE TEXTURIZING

## FINAL REPORT

July 1979

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Gregory T. Jones and Sang S. Rhee

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Sensor Technology, Inc.
21012 Lassen St.
Chatsworth, Ca. 91311

The JPL Low-Cost Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

## PREFACE

The information presented in this report on silicon wafer surface texturizing represents the work performed from December 14, 1978 through July 31, 1979 by Sensor Technology, Inc., in Chatsworth, California. The program was directed by Sang S. Rhee. Contributors to this work include: Gregory T. Jones, Sang S. Rhee, Sanjeev R. Chitre and Kimberly L. Allison.

The JPL technical program manager was David Moffett.

# ABSTRACT

An in-depth study of silicon wafer surface texturizing was conducted in this program. The work discussed in this final report covers four tasks. Task (1) investigated a low-cost cleaning method that utilized recycled Freon in an ultrasonic vapor degreaser to remove organic and inorganic contaminants from the surface of silicon wafers as received from silicon suppliers. Task (2) demonstrated the use of clean dry air and high throughput wafer batch drying techniques to lower the cost of wafer drying. Task (3) examined the two stage texturizing process for suitability in large scale production. Task (4) performed an in-depth gettering study with the two stage texturizing process for the enhancement of solar cell efficiency, minimization of I-V curve dispersion, and improvement in process reproducability.

The 10% efficiency improvement goal was exceeded for the wafer surface texturizing study for the near term implementation of flat plate photovoltaic cost reduction. Production solar cells were produced with 18.3% higher efficiencies than similar solar cells without texturization.

Gettering in combination with a two-stage texturizing process had a significant effect on solar cell batch electrical performance. An 11.8% average batch efficiency improvement was observed for low temperature intermediate gettered solar cells over texturized (no gettering) solar cells.

The wafer cleaning cost reduction goal for the wafer surface texturizing study was achieved. The cleaning materials cost was reduced from 3.7 cents per peak watt (1975 cents) to less than 0.7 cents per peak watt.

The texturizing process cost including cleaning, drying, and texturizing, amounted to 1.26 cents per peak watt. The gettering cost, which used recycled $POCl_3$, was found to be .97 cents per peak watt. These costs are in line with the 1986 DOE/JPL Low-Cost Solar Array Project goal.

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# INTRODUCTION

Initial work on the silicon wafer surface texturizing for the improvement of solar cell efficiency by Sensor Technology was performed under ERDA/JPL Contract No. 954605 (1) under the title "Development of Low-Cost, High Energy-Per-Unit-Area Solar Cell Modules". It was concluded from this program that solar cell efficiencies undergo a definite improvement using the texturizing process. A high degree of consistency and reproducibility was achieved, thus making the process suitable for production.

The texturizing process was manually operated and consisted of five steps. They are: (1) wafer surface cleaning, (2) surface texturizing, (3) four stage cascade rinse, (4) final cleaning and (5) final rinse/spin dry.

The total process cost accumulated during this multi-step manual procedure is 18.15 cents per peak watt in 1975 cents.* The total automated process

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* Recently DOE chose the base year 1980. All cost in this report can be converted to 1980 cents by multiplying the 1975 costs by the conversion factor 1.40.

cost,** which includes the replacement of the rinse/spin dryer with a conveyorized forced clean air dryer tunnel system, is 6.39 cents per peak watt.

The reductions in labor and material costs by automation were considerable but further reductions are necessary in order to meet the 1986 JPL/LSA price goal, which is set at 50 cents per peak watt in 1975 cents for the completed solar cell module. It is estimated that the silicon wafer surface texturizing process costs will have to be reduced to less than 2 cents per peak watt to be in line with the 1986 JPL/LSA price goal.

The general approach of this program is to reduce the cost of the wafer surface texturizing process which includes the cleaning, rinsing, and drying operations of silicon wafers as received from manufacturers, and to develop a two stage texturizing process with gettering to enhance the solar cell efficiency.

The specific goals for this study of wafer surface texturizing for near term implementation of flat plate photovoltaic cost reductions are: (1) Reduce

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** The automated process study was performed by Sensor Technology under DOE/JPL Contract No. 954865 under the title "Phase 2 Array Automated Assembly Task," Quarterly Technical Report. No. 2, March 1978.

the cleaning materials cost from 3.7 cents per peak watt to less than 0.7 cents per peak watt, and (2) produce production solar cells with 10% higher efficiencies than similar solar cells without texturization.

The work in this program was performed in four tasks. Task (1) investigated a low-cost cleaning method to remove organic and inorganic contaminants from the surface of silicon wafers as received from the silicon suppliers. Task (2) involved the use of clean dry air and high throughput wafer batch drying techniques to lower the cost of wafer drying. Task (3) examined the two stage texturizing process for suitability in large scale production. Task (4) performed an in-depth gettering study with the two stage texturizing process for the enhancement of solar cell efficiency, minimization of I-V curve dispersion, and improvement in process reproducability.

All the tasks were performed on a production scale as opposed to a laboratory scale. Production equipment was utilized throughout the investigations. The data was examined primarily to determine general trends and process characteristics which are applicable for near term implementation in large scale production.

## TECHNICAL DISCUSSION

### TASK (1) LOW COST WAFER CLEANING

The major objective of the cleaning process is to remove organic and inorganic surface contaminants from silicon wafers received directly from the wafer manufacturer. Conventional wet chemical cleaning techniques which utilize trichloroethylene or methanol are not cost effective in meeting the 1986 LSA price goals. In view of this circumstance, wafer surface cleaning with recycled Freon TMS was pursued as a candidate procedure for low cost wafer cleaning.

The technology required for Freon TMS recycling is well developed. A model DS-10R-3 Ultrasonic Vapor Degreaser manufactured by Delta Sonics in Long Beach, California, was selected on the basis of performance, capability and cost. The schematic diagram of this equipment is shown in Figure 1. The major system components include an ultrasonic processing tank, two boiling tanks, and a vapor zone. The cleaning chemical (Freon) is boiled in the boiling tank (2), with a submerged heater. A condensor coil in the vapor zone condenses the vapor, which is subsequently collected at the water separator. The water separator separates the water from the chemical solvent, which is then pumped into the ultrasonic tank through a filter. The chemical solvent

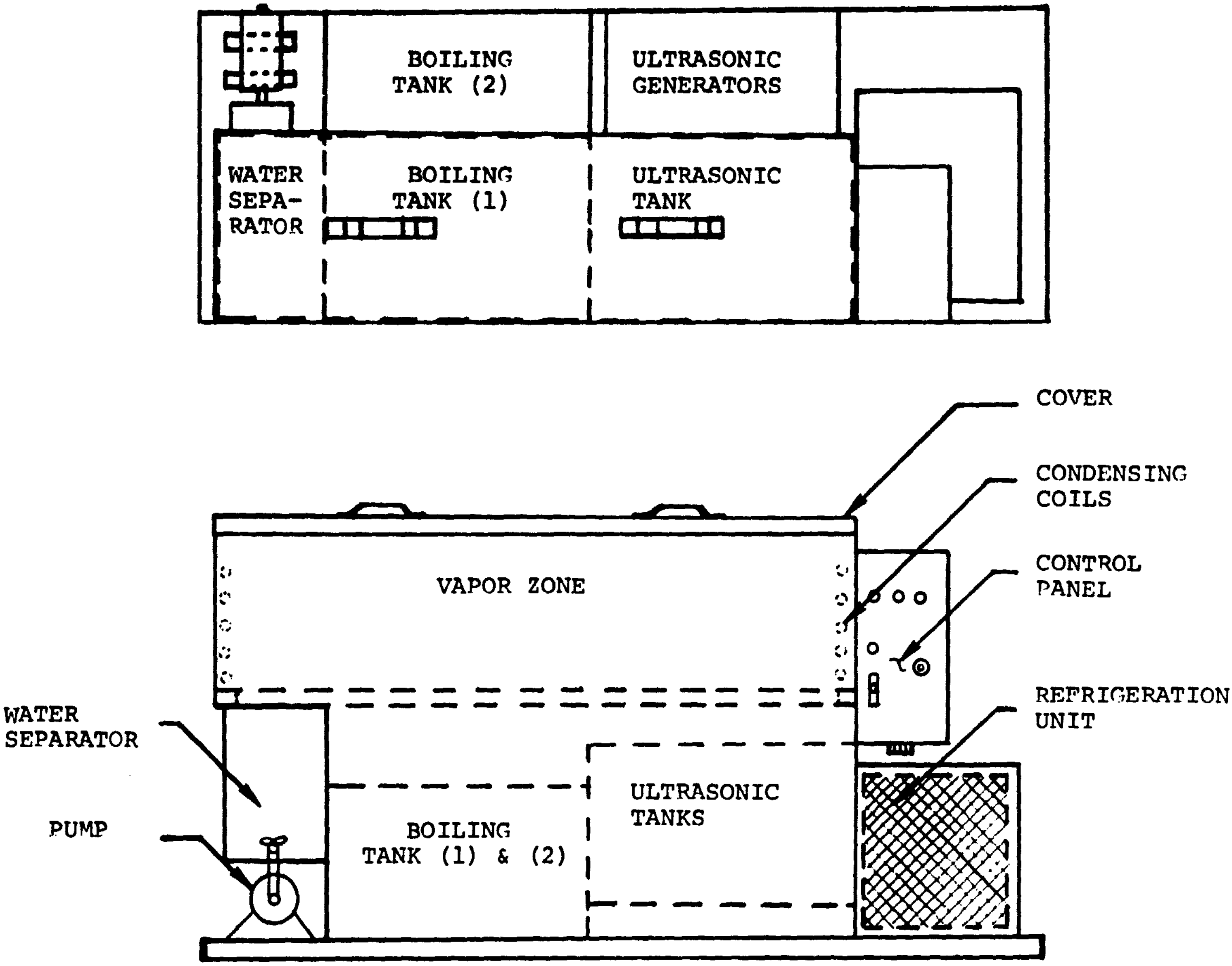


FIGURE 1. SCHEMATIC DIAGRAM OF DELTA SONIC'S ULTRASONIC VAPOR DEGREASER. MODEL NO. 10R-3

will consecutively flow through boiling tanks (1) and (2), since these tanks are constructed as a cascade system.

The performance of the ultrasonic vapor degreaser was verified by running multiple batches of wafers through the sequence and checking the product for both cleanliness and electrical characteristics. They were found to be comparable to wafers processed by conventional wet chemical techniques. The system has now been incorporated into the standard production line because of the results of these tests. To verify the cost effectiveness of wafer cleaning with Freon TMS recycling, an in-depth SAMICS cost analysis was performed for this process and is presented in the section on Process/Equipment Cost Analysis.

## TASK (2) LOW COST WAFER DRYING

The objective of this task is to lower the cost of wafer drying by: (1) using low cost clean air drying and (2) using high throughput wafer batch drying.

### a) Low Cost Clean Air Drying

A clean air drying method was investigated in an effort to reduce the wafer drying cost by replacing dry nitrogen, an expensive inert gas, with filtered dry air. The wafer drying equipment utilized in this task consisted of two components. The first component is an air cleaning unit that reduces the moisture content of the air and filters dust particles. The second component is an experimental wafer drying system which dries wafers by means of an air jet.

A refrigerated air dryer and air line filter manufactured by Arrow Pneumatics, Inc., Mundelein, Illinois were selected for supplying clean compressed air to the wafer drying system. The dryer is model no. A-50 with a 50 SCFM capacity using an R-12 refrigerant and a maximum working pressure of 175 psi. The filter is model no. Oilescer-3308 with a particle size limit of 0.01 micron and a maximum pressure drop at 50 psi. of 2 psi.

A special feature of the Arrow system is a patented tube in the main heater exchanger tube, which contains an inner finned tubing to create turbulence for heat transfer and self cleaning action. The use of the Arrow Refrigerated Air Dryer prior to the use of the Arrow Filter, maximizes the performance and lifetime of the filter element. The primary function of the Arrow Air Filter is to remove harmful contaminants such as condensed moisture, pipe scale, dirt and rust from the incident air stream.

After the system was installed at Sensor Technology, Inc., wafers were processed in large scale production quantities to check the clean air system performance capability. It was demonstrated that the lower-cost clean dry air system can replace the higher cost dry nitrogen system without any observable effects on the solar cell electrical performance.

b) <u>High Throughput Wafer Batch Drying</u>

Two wafer batch drying procedures were examined for high throughput. Both drying procedures involved heating a batch of fifteen three inch diameter wafers in a standard Teflon carrier in D.I. water to a designated temperature followed by removal for drying onto a clean table top. The drying methods differed in that the first method used natural air

convection drying and the second method used forced hot air drying. The investigation was carried out with surface etched and texturized silicon wafers.

The natural air convection drying experiments led to the following temperature versus time observations. At an initial wafer temperature of 95°C (the wafers were removed from the D.I. water bath at 95°C) the surface etched and texturized silicon wafers dried in twenty-three minutes and nine minutes respectively. No indication of spotting was observed on the wafer surfaces. At an initial wafer temperature of 85°C the surface etched and texturized wafers showed evidence of residual water droplets after a time of 35 minutes. It is apparent from these experiments that natural air convection drying is not cost effective due to the long drying time required.

Forced air blow drying experiments were performed in order to see if a low cost high throughput wafer drying method was feasible. A Dayton heat gun, model no. 2Z387 was used to simulate a forced air drying tunnel system. The heat gun is rated for a flow rate of 18.5 CFM at 150°C and an air speed of 1200 feet per minute.

The results of the forced air drying experiments are given in Figure 2. This method was found to dry the silicon wafers completely down to a temperature of 65$^{\circ}$C. A forced air drying tunnel system was found to be cost effective at an initial wafer temperature of 80$^{\circ}$C. A cost analysis on wafer drying is presented in the section on Process/ Equipment Cost Analysis.

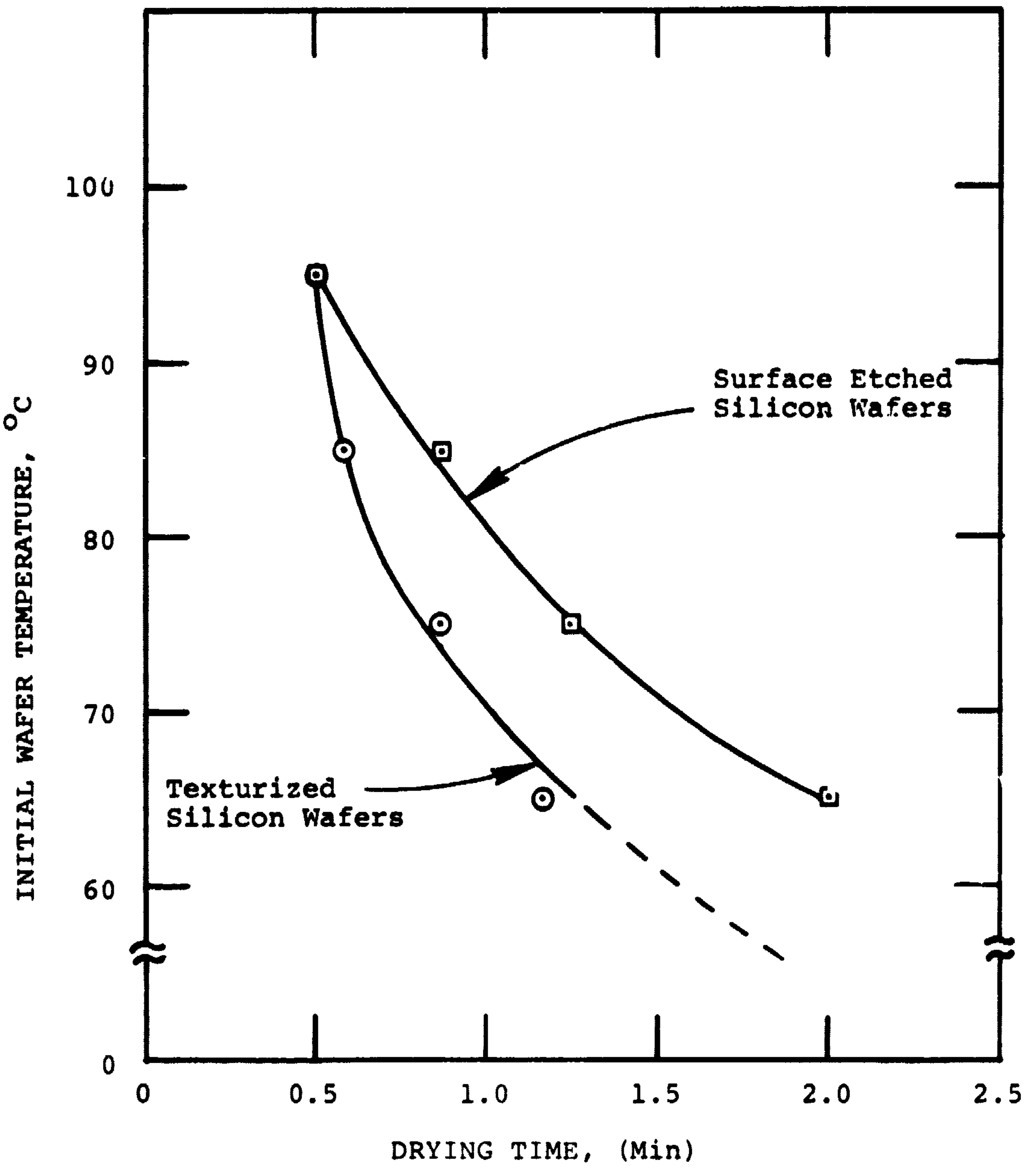


Figure 2. Forced air drying experimental results; initial wafer temperature versus drying time for three inch diameter silicon wafers.

## TASK (3) TWO-STAGE TEXTURIZING PROCESS

Wafer surface texturizing involves the use of orientation dependant etches that reduce front surface solar cell reflection losses. The surface macrostructures produced by anisotropic sodium hydroxide etching have been found to significantly improve solar cell photovoltaic energy conversion efficiency. [1-8]

A two-stage texturizing process was developed which utilizes two NaOH and D.I. water etching solutions consisting of 10% NaOH by weight to D.I. water and 1% NaOH by weight to D.I. water, respectively. [1] Under laboratory conditions, where the initial wafer surface characteristics, i.e. surface contaminants, saw marks and chips are controlled, the processing time for each step was found to be five minutes. These wafers are typical of those received from a single supplier and are not severely contaminated or surface damaged.

In large scale production, where currently the wafer surface characteristics are not controlled, the processing time was found to be variable and to require more than five minutes for each etching step. These wafers are typically received from more than one supplier and may have surfaces which are severely contaminated and damaged.

Silicon wafers, which were cleaned by the low-cost cleaning process in Task 1, developed uniform surface macrostructures after undergoing the two-stage texturization process. However, an optimum etching time for a given characteristic batch of silicon wafers was not obtained in this task. Analysis of as-cut silicon wafer surface characteristics versus optimum etching time in large scale production is beyond the scope of this program. It is recommended that a study be made on silicon wafer surface characteristics versus etching time in large scale production.

## TASK (4) GETTERING WITH TWO-STAGE TEXTURIZING

The gettering method used in this task consisted of heating silicon wafers in the presence of $POCl_3$ to grow a phosphosilicate glass layer on the silicon surface followed by etching off the glass layer. Phosphosilicate glass gettering has been used for some time to remove unwanted electrically active impurities from silicon wafers.[(9)] It is the purpose of this study to determine whether phosphosilicate glass gettering during solar cell fabrication will serve to improve solar cell efficiencies.

The gettering process as described above, is ideally suited to be performed in conjunction with Sensor Technology's two stage texturization process (see Task 3), since either the one percent or ten percent NaOH etching steps performed in this process sequence would remove the gettered surface. Consequently, a series of experiments were carried out to study the gettering effect in conjunction with the two stage texturizing process on silicon solar cell electrical performance.

The overall program plan for the gettering task had three main objectives, which were: (1) to increase the average gettered solar cell efficiency with respect to the average efficiency of a controlled batch of ungettered solar cells, (2) to minimize the

I-V curve dispersion for any batch of solar cells, and (3) to develop a reproducible gettering process.

The experimental approach in this program was directed toward analysis of five parameters, which are: (1) gettering step placement with respect to the two stage texturizing process, (2) gettering temperature, (3) silicon wafer material quality, (4) silicon wafer size, and (5) recycled gettering.

a) Preliminary Experiments "Series P"

Preliminary experiments were performed to investigate the gettering temperature and placement within the solar cell process. Four sample batches, which are designated "Series P", each consisting of twenty-five 3.35 inch (85mm) diameter silicon wafers were processed. The solar cells were processed with Sensor Technology's standard two stage (10%/1% NaOH) texturizing process sequence, $POCl_3$ diffusion step, electroless nickel plating step, aluminum back surface, solder and no A.R. coating. All solar cells have identical parallel track grid patterns. The solar cells were tested under a tungsten light source (G.E. Quartzline Lamp DWY, 2800°K calibrated at 100 mW/cm$^2$ at 28°C).

Electrical performance data for Batches P-1 through P-4 were determined from the corresponding experimental I-V curves presented in Figures 3 through 6 respectively, and are summarized in Table 1.

Batch P-1 was not gettered and is designated as the control batch. From Figure 3, it is clear that Batch P-1 has a very large efficiency and fill factor dispersion which are designated in Table 1 by $\Delta\eta/\eta$ (%) and $\Delta FF/FF$ (%). The lowest solar cell I-V curve in Figure 3 was not included in the calculations.

Batch P-2 underwent a high temperature ($1000^\circ C$, 35 min) intermediate gettering step (gettering between the 10% NaOH and 1% NaOH steps in the two stage texturizing process sequence). Figure 4 clearly shows that Batch P-2 also has a very large efficiency and fill factor dispersion. However, the average efficiency (a weighted average efficiency) of Batch P-2 is higher than the nongettered Batch P-1.

Batch P-3 was pregettered (gettered prior to the two stage texturizing process) at $875^\circ C$, 35 minutes. The I-V curves for the pregettered solar cells are shown in Figure 5. The average efficiency is higher and the efficiency and fill factor dispersion is smaller than the nongettered control Batch P-1. The pregettered batch is also characterized by two very low I-V curves which were not included in the dispersion calculations.

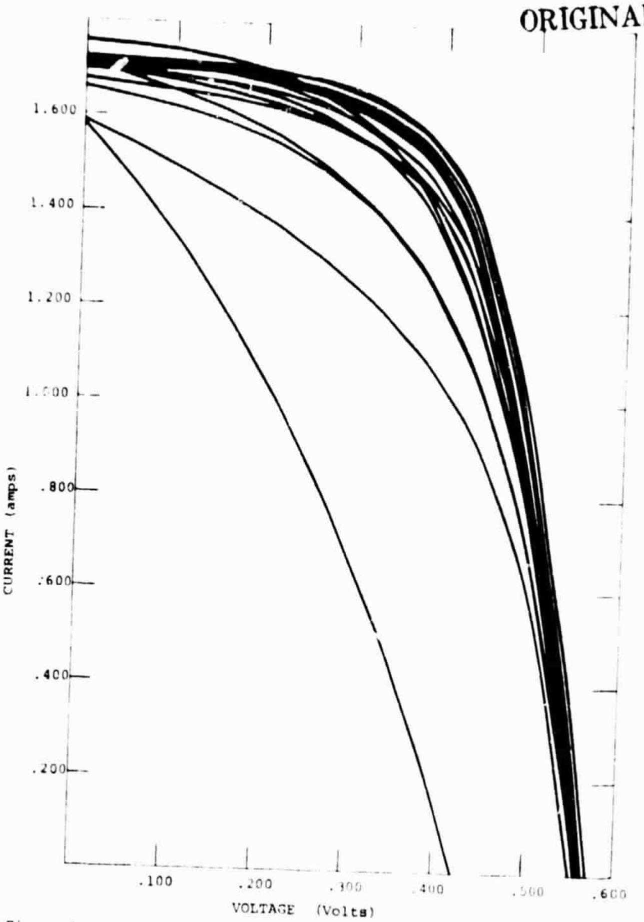


Figure 3: Electrical performance curves for 3.35 inch diameter texturized solar cells, Batch P-1.

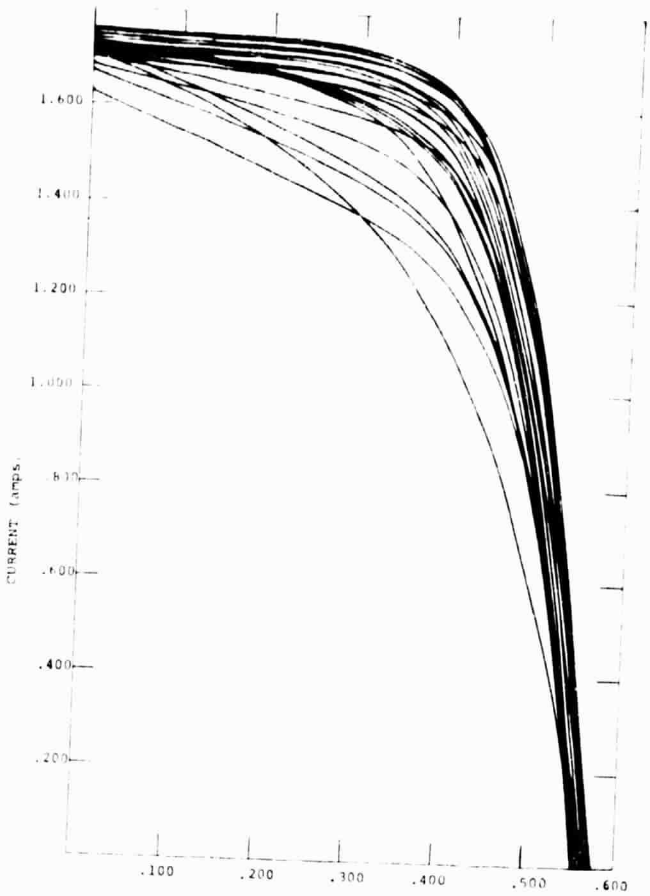


Figure 4: Electrical performance curves for 3.35 inch diameter intermediate gettered ($POCl_3$, 1000°C) solar cells, Batch P-2.

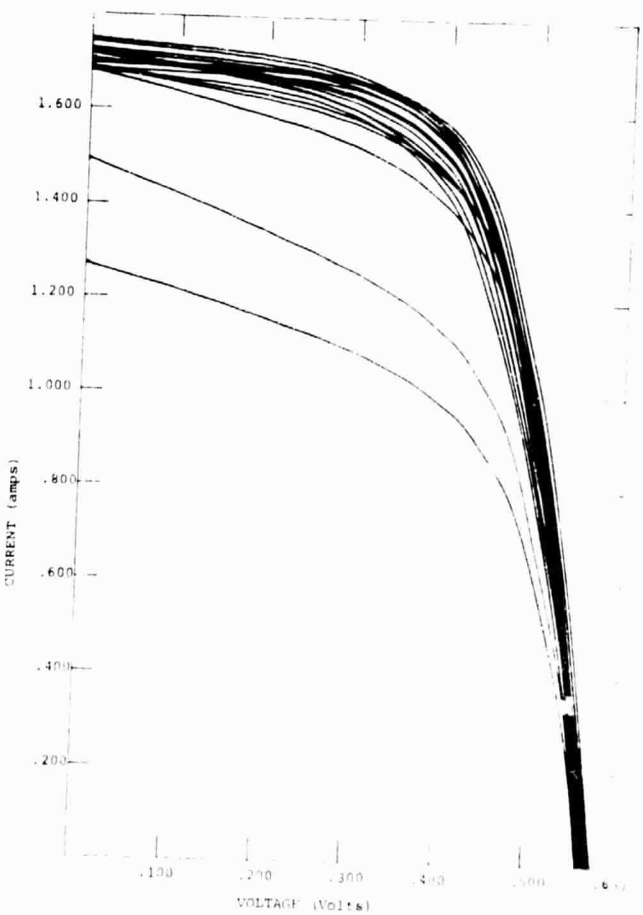


Figure 5: Electrical performance curves for 3.35 inch diameter pregettered ($POCl_3$, 875°C) solar cells, Batch P-3.


Figure 6: Electrical performance curves for 3.35 inch diameter intermediate gettered ($POCl_3$, 875°C) solar cells, Batch P-4.

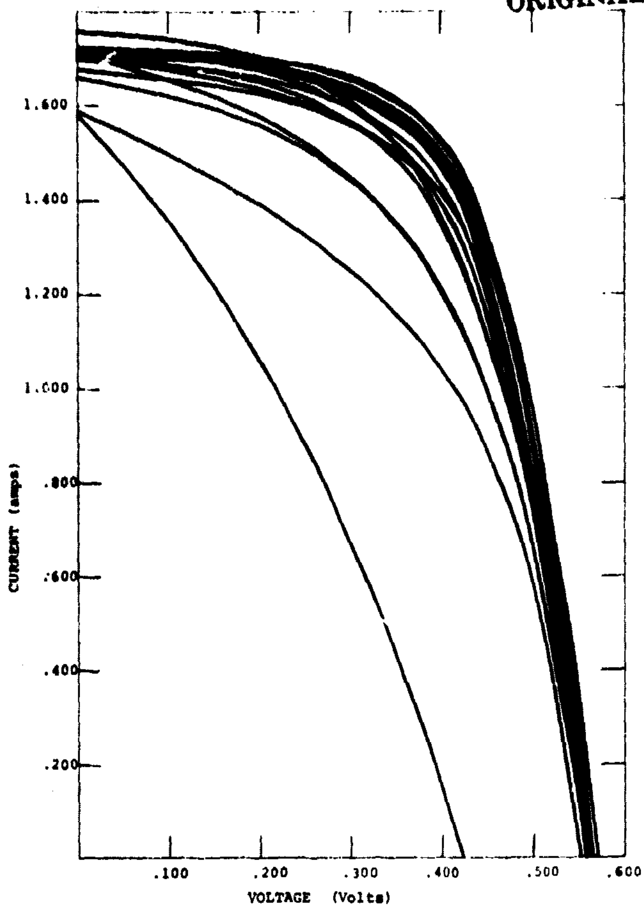


**Figure 3:** Electrical performance curves for 3.35 inch diameter texturized solar cells, Batch P-1.

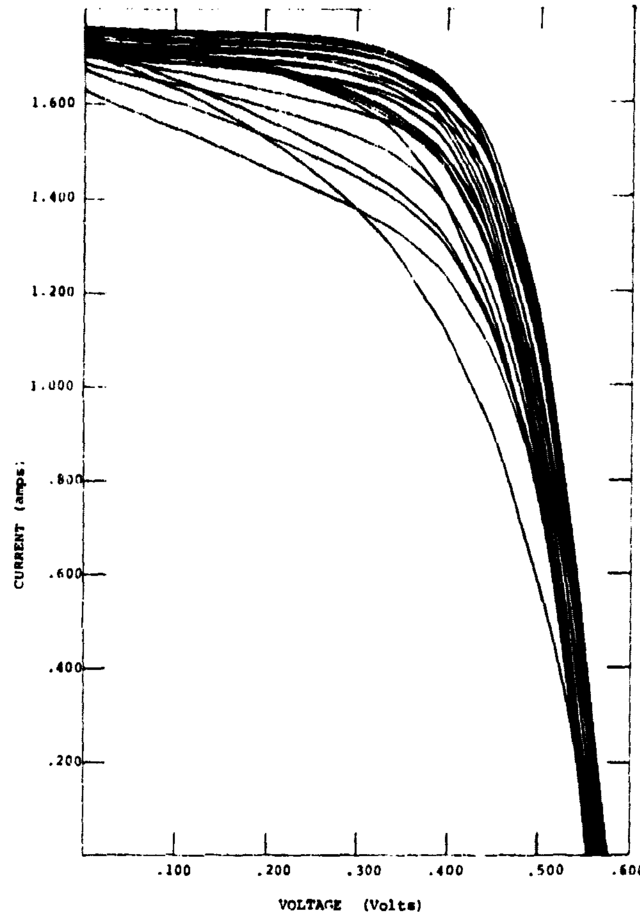


**Figure 4:** Electrical performance curves for 3.35 inch diameter intermediate gettered ($POCl_3$, 1000°C) solar cells, Batch P-2.

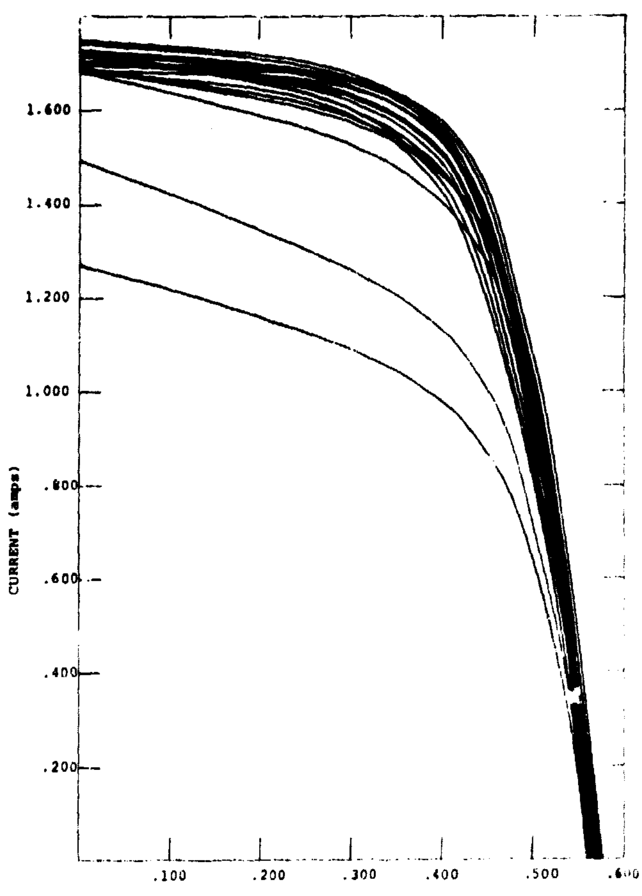


**Figure 5:** Electrical performance curves for 3.35 inch diameter Pregettered ($POCl_3$, 875°C) solar cells, Batch P-3.

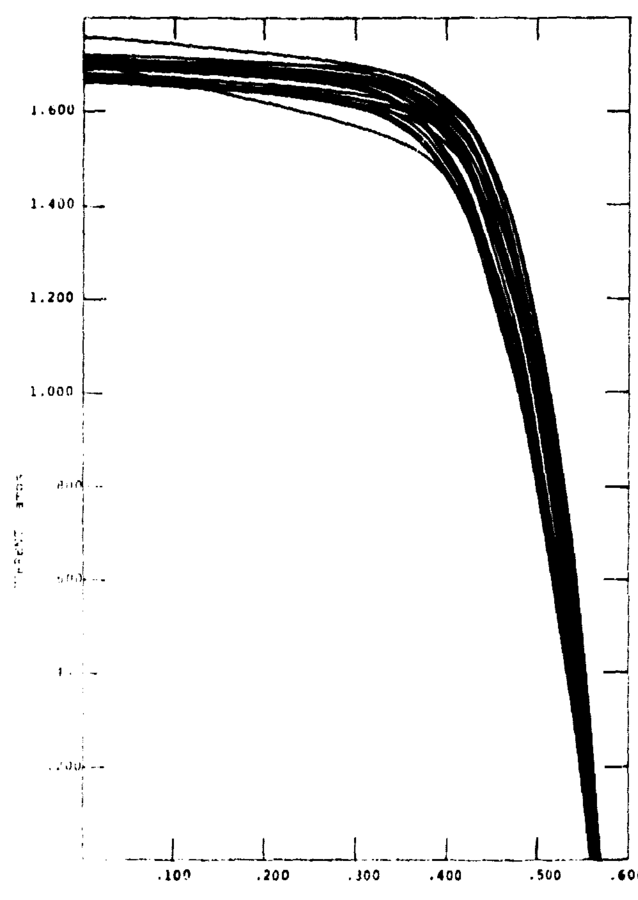


**Figure 6:** Electrical performance curves for 3.35 inch diameter intermediate gettered ($POCl_3$, 875°C) solar cells, Batch P-4.

TABLE 1. SOLAR CELL ELECTRICAL PERFORMANCE RESULTS SHOWING THE EFFECTS OF TEXTURIZING AND GETTERING 3.35 INCH (85MM) DIAMETER SILICON MATERIAL.

| Batch | $I_{sc}$(a) | $V_{oc}$(v) | $I_{pp}$(a) | $V_{pp}$(v) | $\eta$(%) | FF | $\frac{\Delta\eta}{\eta}$(%) | $\frac{\Delta FF}{FF}$(%) |
|---|---|---|---|---|---|---|---|---|
| P-1 | Controlled cell, std. two step. tex., std. $POCl_3$ diff., nickel plated with an aluminum back and no A.R. coating. | | | | | | | |
| High | 1.72 | .570 | 1.46 | .415 | 11.02 | .618 | 10.87 | 6.73 |
| Low | 1.59 | .560 | 1.04 | .400 | 7.56 | .467 | -23.94 | -19.34 |
| Wt. Ave. | 1.67 | .565 | 1.35 | .405 | 9.94 | .579 | | |
| P-2 | Intermediate Gettering (1000°C, 35 min). | | | | | | | |
| High | 1.76 | .570 | 1.59 | .420 | 12.14 | .666 | 10.66 | 7.94 |
| Low | 1.70 | .560 | 1.08 | .400 | 7.85 | .454 | -28.44 | -26.42 |
| Wt. Ave. | 1.73 | .565 | 1.42 | .425 | 10.97 | .617 | | |
| P-3 | Pre-gettering (875°C, 35 min). | | | | | | | |
| High | 1.73 | .580 | 1.54 | .420 | 11.76 | .645 | 7.69 | 5.05 |
| Low | 1.68 | .570 | 1.36 | .420 | 10.39 | .596 | - 4.85 | - 2.93 |
| Wt. Ave. | 1.70 | .575 | 1.43 | .420 | 10.92 | .614 | | |
| P-4 | Intermediate gettering (875°C, 35 min). | | | | | | | |
| High | 1.72 | .575 | 1.55 | .435 | 12.26 | .682 | 5.78 | 3.65 |
| Low | 1.67 | .565 | 1.39 | .425 | 10.74 | .626 | -7.33 | - 4.86 |
| Wt. Ave. | 1.70 | .570 | 1.50 | .425 | 11.59 | .658 | | |

Figure 6 shows the I-V curves from Batch P-4. The solar cells have undergone an intermediate gettering step at 875°C, 35 minutes. The low temperature intermediate gettered solar cells have a significantly higher average efficiency and smaller average efficiency and fill factor dispersion than the nongettered control Batch P-1, the high temperature intermediate gettered Batch P-2, or the low temperature pregettered Batch P-3. The low temperature intermediate gettered solar cells are characterized by very well defined I-V curves and no low efficiency solar cells.

The trends depicted in Table 1 suggest the following preliminary conclusions:

(1) Gettering improves average solar cell efficiencies.

(2) The best solar cell electrical performance for the initial test data takes place with an intermediate gettering step at a temperature of 875°C for 35 minutes. *

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* A thirty-five minute gettering time was utilized for these preliminary experiments and for all other gettering experiments performed in this program. This gettering time was chosen from past experience with $POCl_3$ diffusion.

(3) Low temperature intermediate gettering produces solar cells with very small efficiency and fill factor dispersion. It therefore appears that low temperature intermediate gettering may lead to batch to batch reproducibility.

(b) Quality of Silicon Wafer Material

Additional gettering experiments were performed to evaluate the preliminary conclusions made in the previous section. Low and fair quality silicon wafer material was used in the analysis. In the context of this study, the quality of the silicon material is defined in terms of the electrical performance or characteristic I-V curves for a batch of solar cells. A batch of solar cells is a group of solar cells processed together under (nearly) identical conditions.

Low quality silicon wafer material is characterized by a batch of solar cells with a very large dispersion in short circuit current and photovoltaic energy conversion efficiency. The material may be (but not necessarily be) characterized by a large dispersion in fill factor and a moderately large dispersion in open circuit voltage.

Fair quality silicon wafer material is characterized by a moderate dispersion in short circuit current and a moderately large dispersion in solar cell efficiency and may be (but not necessarily be) characterized by a moderately large dispersion in fill factor and a small dispersion in open circuit voltage.

In the following discussion, low quality silicon wafer material will be designated as "Series A" and the fair quality silicon wafer material will be designated as "Series B". Also, the silicon wafer material designated as "Series P", "Series C" and "Series D" is fair quality material.

(c) <u>Low Quality Silicon Wafers "Series A"</u>

A gettering study was made on low quality Czochralski, as cut silicon wafers. Four batches, which are designated "Series A", each consisting of twenty-five 1.406 inch (35.7mm) square silicon wafers were processed with Sensor Technology's two stage (10%/1% NaOH) texturizing process sequence, spray-on dopant junction formation ($n^+$ front surface and $p^+$ back surface), electroless nickel plating step, aluminum back surface, solder coating step, and no A.R. coating. These silicon wafers were laserscribed (scribed then manually broken) from 2.25 inch (64mm) diameter round silicon wafers. The parallel track gridline pattern for the square solar cells was not optimized.

Electrical performance data for Batches A-1 through A-4 were determined from the corresponding experimental I-V curves presented in Figure 7 through 10 respectively, and are summarized in Table 2. The batches are differentiated on the basis of the location of the gettering step with respect to the two step texturizing process. Batch A-1 was not gettered and is the control batch.

The I-V curves for Batch A-2 which was not gettered but underwent $SiO_2$ removal are shown in Figure 8. Batch A-2 shows a slight improvement in average photovoltaic energy conversion efficiency relative to the control batch. Batch A-2 has a large efficiency and fill factor dispersion.

Figure 9 shows the I-V curves of Batch A-3 which was gettered (875$^{o}$C, 35 min) prior to texturization. Batch A-3 shows a decrease in efficiency and fill factor dispersion relative to the control batch, as well as a relative improvement in average photovoltaic energy conversion efficiency.

Batch A-4, Figure 10, underwent intermediate gettering (875$^{o}$C, 35 min.). Batch A-4 displays, by far, the narrowest efficiency and fill factor dispersion of all four batches, as well as the highest average efficiency.

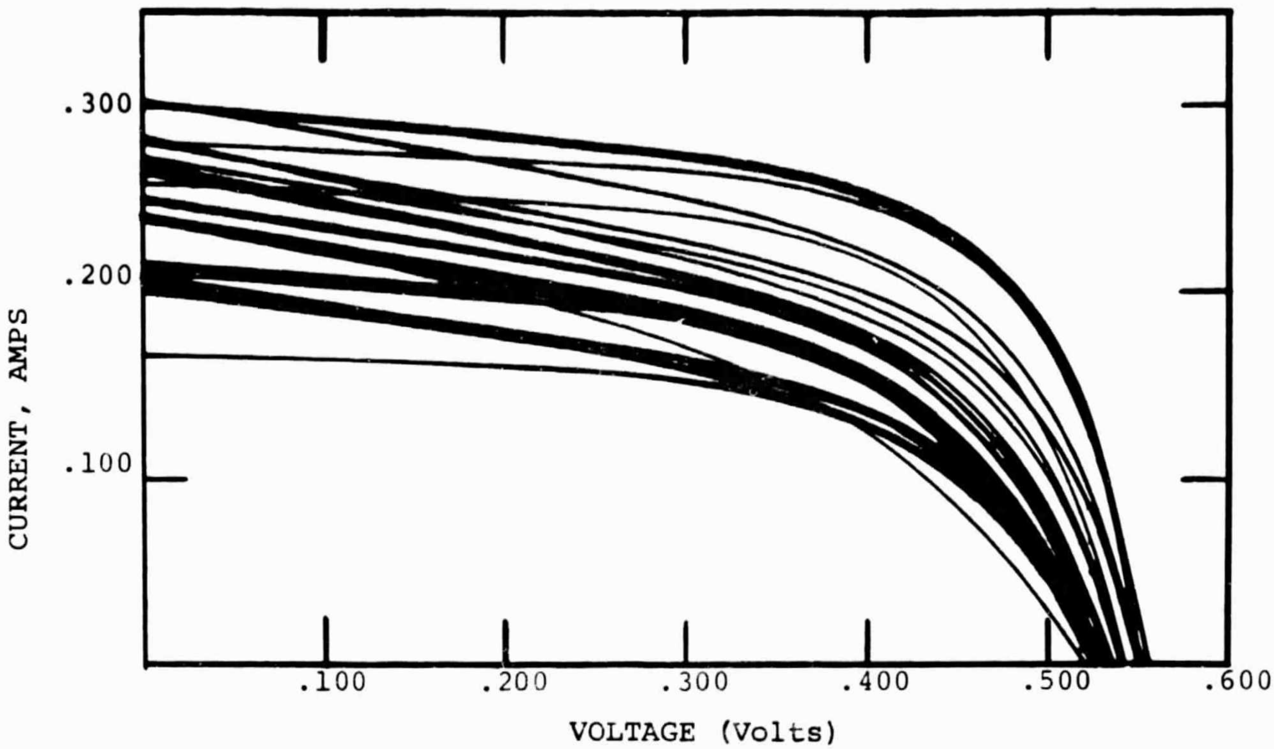


Figure 7: Electrical performance curves for 1.406 inch square texturized, spray-on doped solar cells, Control Batch A-1.

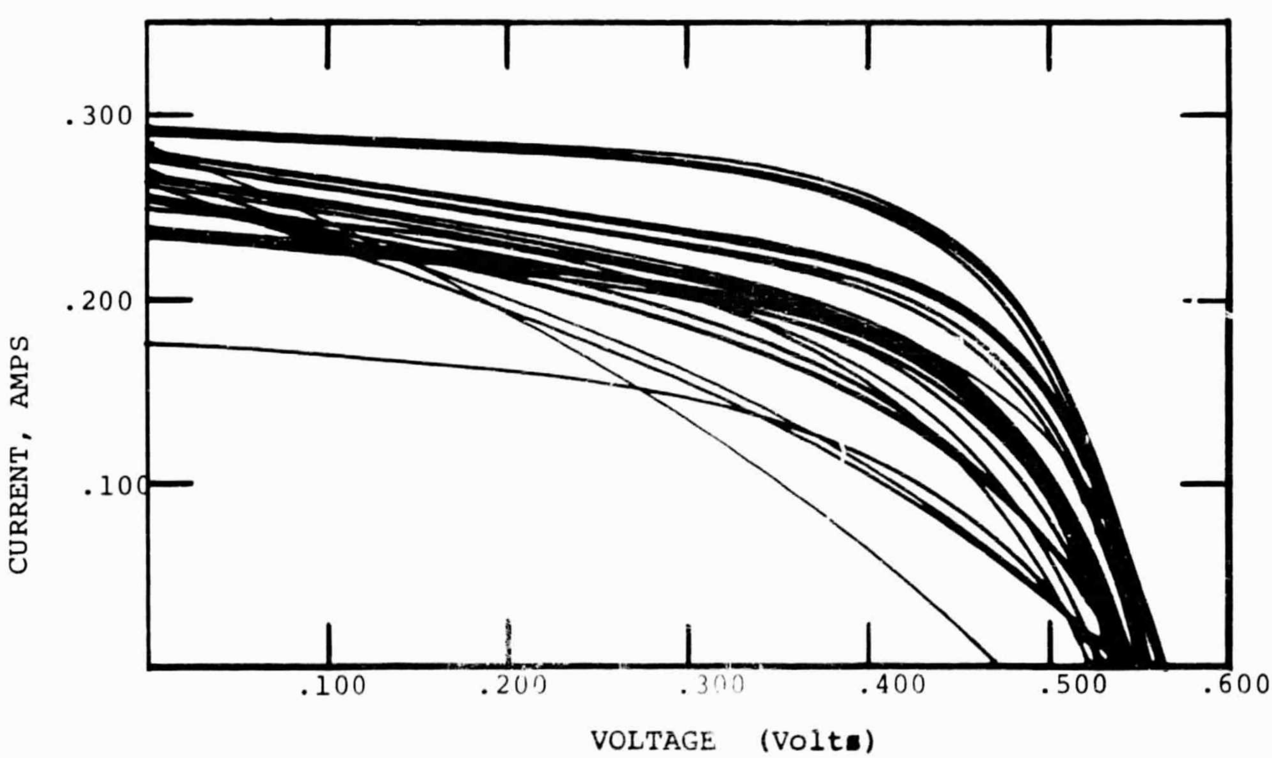


Figure 8: Electrical performance curves for 1.406 inch square texturized, spray-on doped solar cells with $SiO_2$ glass removed, Batch A-2.

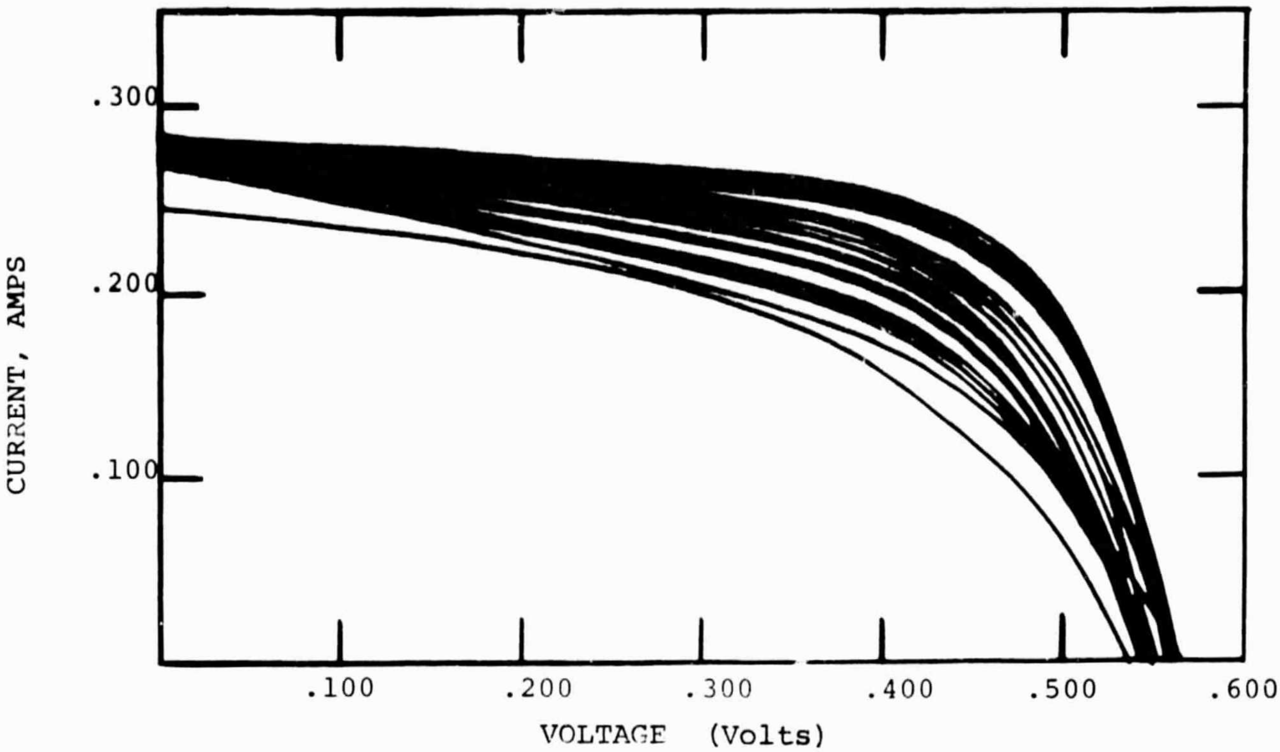


Figure 9: Electrical performance for 1.406 inch square pregettered ($POCl_3$, 875°C) spray-on doped solar cells, Batch A-3.

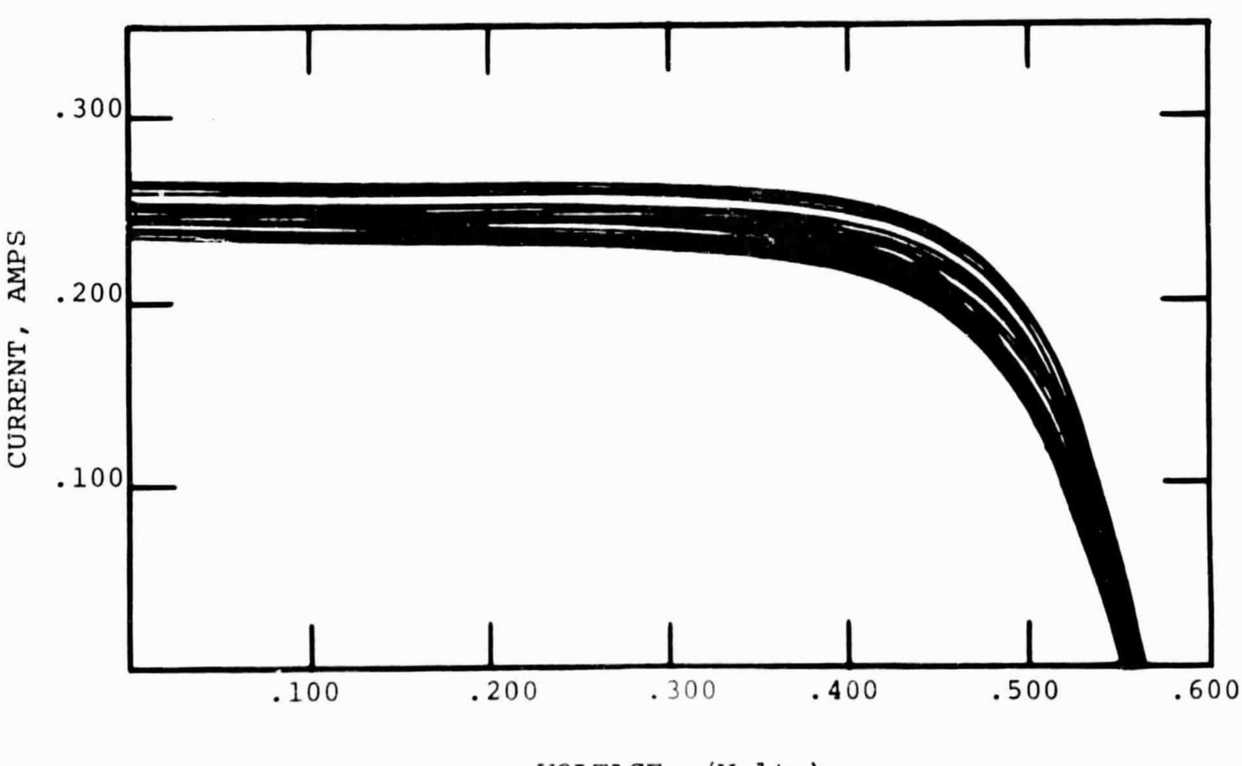


Figure 10: Electrical performance curves for 1.406 inch square intermediate gettered ($POCl_3$, 875°C) spray-on doped solar cells, Batch A-4.

Table 2. Solar cell electrical performance results on the effect of gettering and texturizing on low quality 1.406 inch, square silicon material.

| BATCH | $I_{sc}$ (a) | $V_{oc}$ (v) | $I_{pp}$ (a) | $V_{pp}$ (v) | $\eta$ (%) | FF | $\frac{\Delta\eta}{\eta}$ (%) | $\frac{\Delta FF}{FF}$ (%) |
|---|---|---|---|---|---|---|---|---|
| A-1 Solar Cells: 1.406 inch square, texturized (10%, NaOH), texturized (1% NaOH), spray-on doped (both sides), nickel plated, no A.R. coating. | | | | | | | | |
| High | .300 | .550 | .235 | .450 | 8.30 | .640 | +56.6 | +24.3 |
| Low | .200 | .520 | .105 | .450 | 3.70 | .450 | -30.2 | -12.6 |
| Wt.Ave. | .245 | .535 | .150 | .450 | 5.30 | .515 | -- | -- |
| A-2 Solar Cells: 1.406 inch square, texturized (10% NaOH) texturized (1% NaOH) spray-on doped (both sides, nickel plated, $SiO_2$ glass removed | | | | | | | | |
| High | .290 | .550 | .235 | .450 | 8.28 | .663 | +46.3 | -18.4 |
| Low | .235 | .515 | .100 | .400 | 3.14 | .330 | -44.5 | -37.7 |
| Wt.Ave. | .255 | .535 | .170 | .425 | 5.66 | .530 | -- | -- |
| A-3 Solar Cells: 1.406 inch square, gettered, texturized (10% NaOH), texturized (1% NaOH), spray-on doped (both sides) Nickel plated, no A.R.coating. | | | | | | | | |
| High | .285 | .560 | .235 | .455 | 8.38 | .670 | +18.9 | +13.6 |
| Low | .267 | .535 | .155 | .400 | 4.85 | .430 | -31.2 | -27.1 |
| Wt.Ave. | .280 | .545 | .200 | .450 | 7.05 | .590 | -- | -- |
| A-4 Solar Cells: 1.406 inch square, texturized (10% NaOH), gettered, texturized (1% NaOH), spray-on doped (both sides), nickel plated, no A.R.coating. | | | | | | | | |
| High | .260 | .565 | .230 | .465 | 8.38 | .730 | +8.0 | +2.8 |
| Low | .235 | .555 | .195 | .450 | 6.90 | .680 | -11.1 | -3.8 |
| Wt.Ave. | .250 | .560 | .220 | .450 | 7.76 | .707 | -- | -- |

The effect of SiO anti-reflective coating in conjunction with intermediate gettering is shown in Figure 11 and in Table 3. The lower set of curves in the figure correspond to Batch A-4 which had undergone an intermediate gettering step at 875°C, but no A.R. coating. The upper set of curves in the figure correspond to Batch A-5 which had undergone an intermediate gettering step at 875°C for 35 minutes and SiO A.R.coating. Although both batches display a narrow efficiency and fill factor dispersion, the average efficiency of Batch A-5 with SiO A.R. coating is 21.46% higher than Batch A-4 without an A.R.coating.

A batch of solar cells, which underwent a $POCl_3$ diffusion step instead of the spray-on dopant junction formation step, was processed and tested for comparison with the spray-on doped solar cells. Batch A-6 consisting of twenty-five 1.406 inch (35.7 mm) square silicon wafers was processed with Sensor Technology's two stage texturizing process sequence with no gettering step, $POCl_3$ diffusion step with no p+ back surface field, electroless nickel plating, aluminum back surface, solder and SiO A.R.coating. The electrical performance of Batch A-6 is shown in Figure 12 and is summarized in Table 3. The batch displays a low average efficiency with high efficiency and fill factor dispersion.

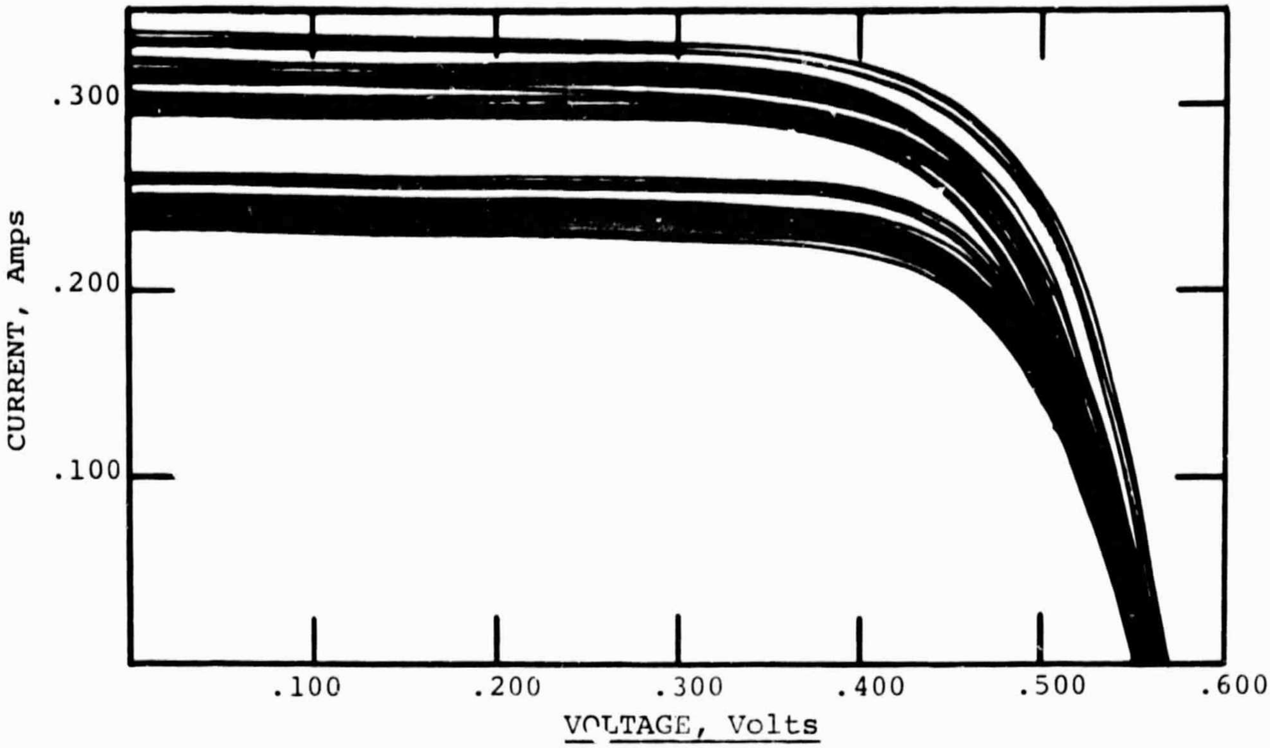


Figure 11. Electrical performance curves for 1.406 inch square intermediate gettered ($POCl_3$, 875°C) spray-on doped solar cells with and without SiO A.R. coating, Batch A-5.

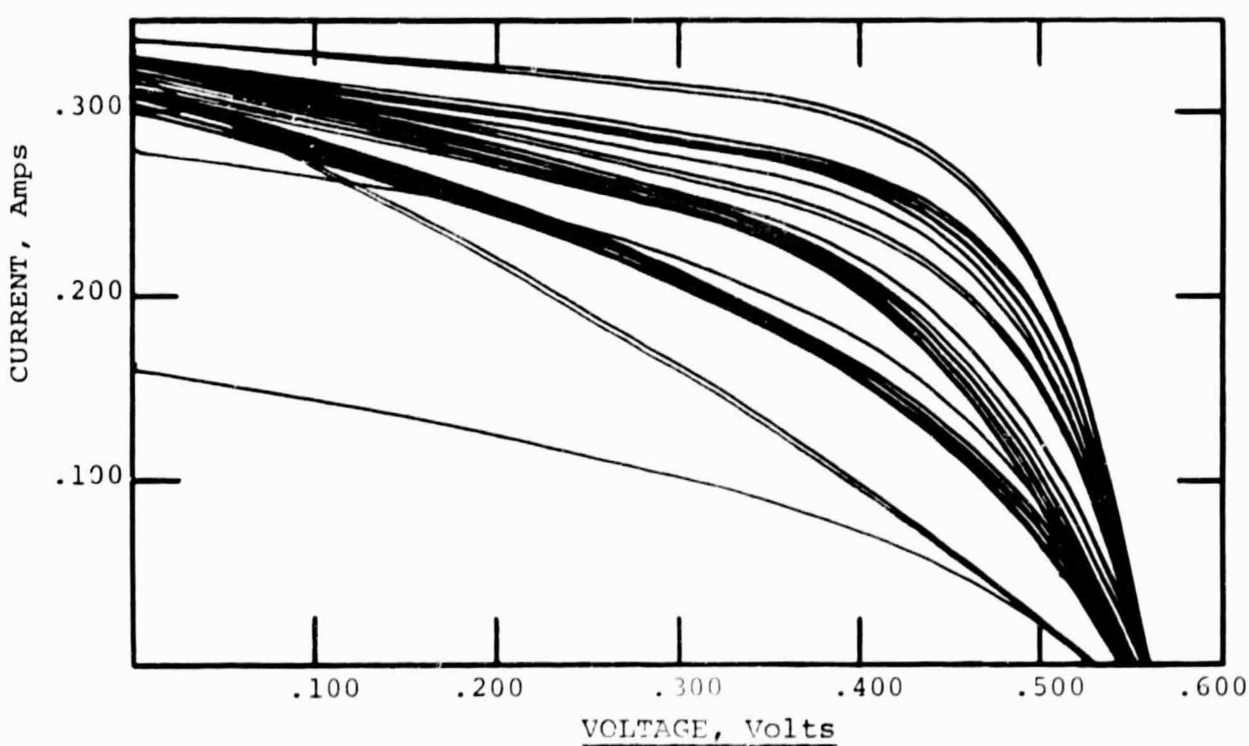


Figure 12. Electrical performance curves for 1.406 inch square texturized, $POCl_3$ diffused solar cells, Batch A-6.

Table 3. Solar cell electrical performance results on the effect of gettering, texturizing and A.R.Coating on low quality 1.406 inch, square silicon material.

| BATCH | $I_{SC}$(a) | $V_{OC}$(v) | $I_{pp}$(a) | $V_{pp}$(v) | $\eta$(%) | FF | $\frac{\Delta\eta}{\eta}$(%) | $\frac{\Delta FF}{FF}$(%) |
|---|---|---|---|---|---|---|---|---|
| A - 4 Intermediate gettering, spray-on doped (both sides) | | | | | | | | |
| High | .260 | .565 | .23 | .465 | 8.38 | .73 | + 8.0 | + 2.8 |
| Low | .235 | .555 | .195 | .45 | 6.90 | .68 | -11.1 | - 4.2 |
| Wt.Ave. | .250 | .560 | .22 | .45 | 7.76 | .71 | | |
| A - 5 Intermediate gettering, spray-on doped (both sides), SiO.A.R. coating | | | | | | | | |
| High | .330 | .570 | .300 | .450 | 10.58 | .72 | + 7.1 | + 1.4 |
| Low | .295 | .555 | .255 | .450 | 8.99 | .70 | - 9.0 | - 1.4 |
| Wt. Ave. | .315 | .563 | .280 | .450 | 9.88 | .71 | | |
| A - 6 No gettering, $POCl_3$ diffusion, SiO A.R.coating | | | | | | | | |
| High | .335 | .565 | .265 | .460 | 9.55 | .64 | +50.6 | +39.1 |
| Low | .160 | .520 | .075 | .400 | 2.35 | .36 | -62.9 | -21.7 |
| Wt.Ave. | .320 | .545 | .180 | .450 | 6.34 | .46 | | |

From the preceding discussion, it is clear that low temperature intermediate gettering in conjunction with the $SiO_2$ glass removed and with an A.R. coating (SiO) applied led to a higher average solar cell efficiency and lower efficiency and fill factor dispersion than ungettered or pregettered solar cells. A large improvement in average solar cell efficiency can be achieved using low temperature intermediate gettering for low quality silicon. The electrical performance of solar cells, which have been texturized and spray-on doped, but not gettered, is very similar to the electrical performance of solar cells which have been texturized and $POCl_3$ diffused but not gettered. The spray-on doped solar cells, which were processed with a low temperature gettering step, had significantly higher average efficiency and small efficiency and fill factor dispersion than the diffused solar cells which were processed without a gettering step.

(d) Fair Quality Silicon Wafers "Series B"

A gettering study was made on fair quality Czochralski, as cut silicon wafers. Four batches, which are designated "Series B", each consisting of twenty-five three inch (76mm) diameter silicon wafers were processed with the same Sensor Technology process as given in Task 4 (a).

Electrical performance data for Batches B-1 through B-4 were determined from the corresponding experimental I-V curves presented in Figures 13 through 16 respectively, and are summarized in Table 4. The batches are differentiated on the basis of the location of the gettering step with respect to the two step texturizing process.

Batch B-1 was not gettered and is the control batch. Figure 13 shows the large efficiency dispersion of the control cells.

Figure 14 shows the I-V curves from Batch B-2. The solar cells have undergone an intermediate gettering step at 875°C for 35 minutes. Batch B-2 has a significantly higher average efficiency and small efficiency and fill factor dispersion than the control Batch B-1.

Figure 15 shows the I-V curves from Batch B-3 which was pregettered at 875°C for 35 minutes. The average efficiency is higher and the efficiency and fill factor dispersion is smaller than the non-gettered control Batch B-1. The average efficiency is lower and the efficiency and fill factor dispersion is slightly larger than the intermediate gettered Batch B-2 solar cells.

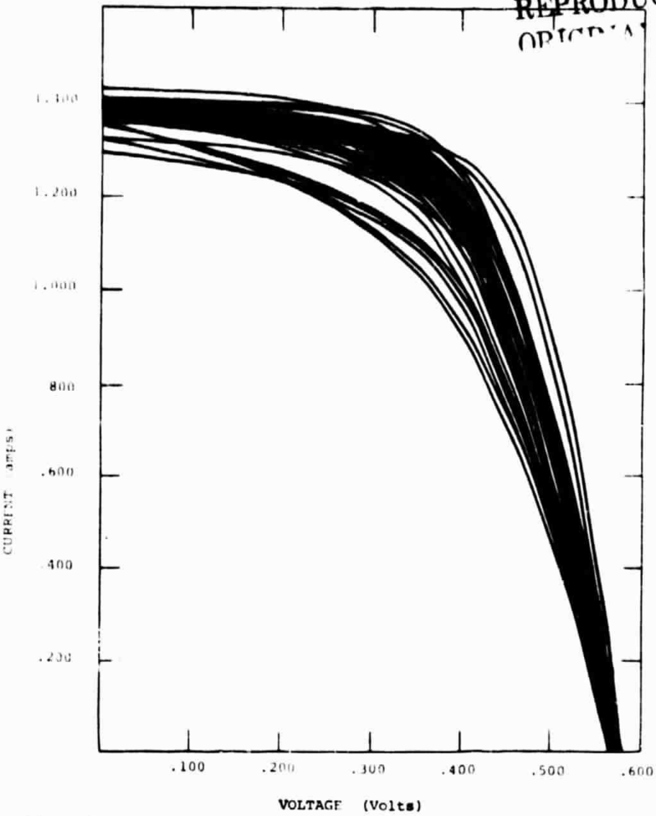


**Figure 13:** Electrical performance curves for 3 inch diameter texturized solar cells, control Batch B-1.

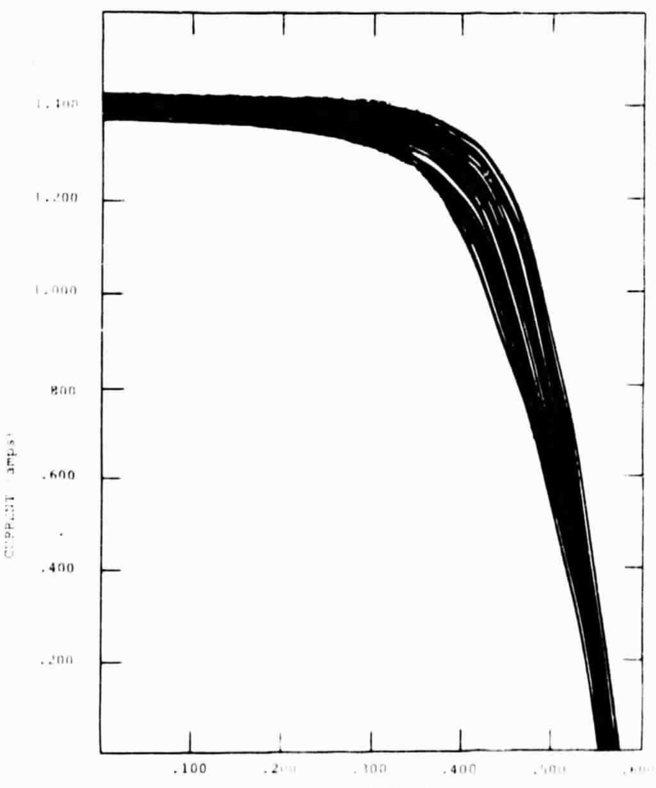


**Figure 14:** Electrical performance curves for 3 inch diameter intermediate gettered ($POCl_3$, 875°C) solar cells, Batch B-2.

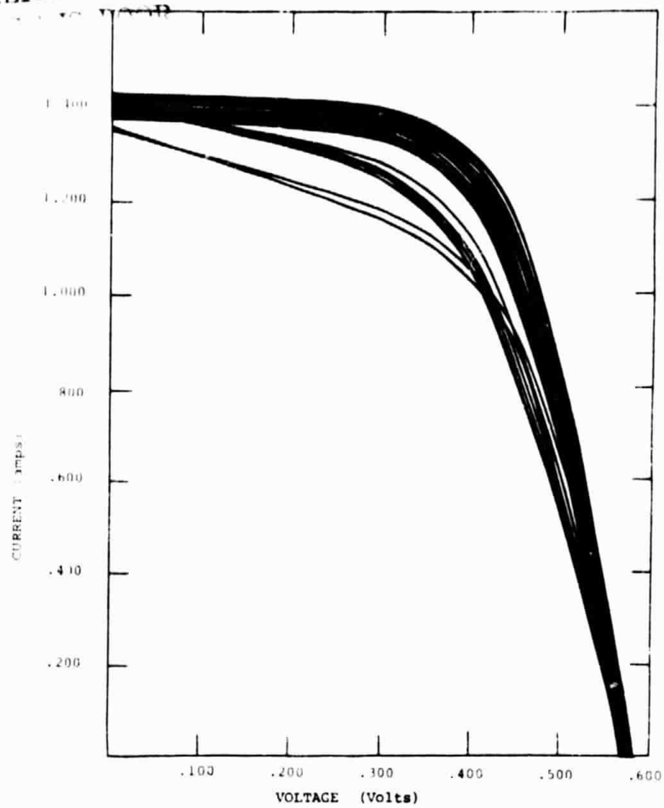


**Figure 15:** Electrical performance curves for 3 inch diameter pre-gettered ($POCl_3$, 875°C) solar cells, Batch B-3.

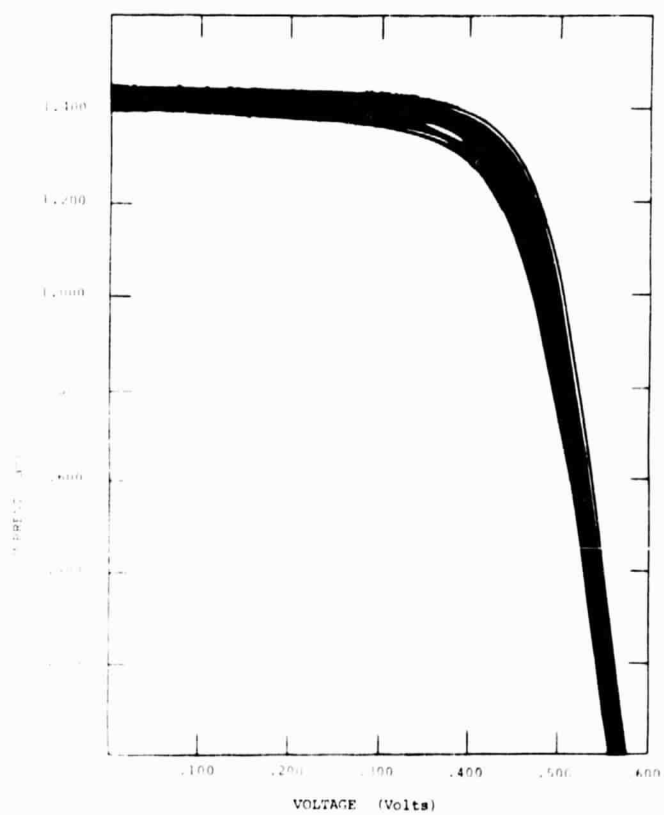


Figure 16: Electrical performance curves for 3 inch diameter intermediate gettered ($POCl_3$, 875°C) solar cells with SiO A.R. coating, Batch B-4.

Table 4. Solar cell electrical performance results on the effects of gettering and texturizing on good quality 3 inch diameter round silicon material.

| Batch | Isc (A) | Voc (V) | Ipp (a) | Vpp (v) | $\eta$ (%) | FF | $\frac{\Delta\eta}{\eta}$ (%) | $\frac{\Delta FF}{FF}$ (%) |
|---|---|---|---|---|---|---|---|---|
| B-1. Controlled Cell, Std. Two Step Tex., Std. $POCl_3$ Diff. with Al Back | | | | | | | | |
| High | 1.40 | 0.580 | 1.22 | 0.435 | 12.82 | 0.654 | 16.55 | 15.14 |
| Low | 1.30 | 0.565 | 0.99 | 0.365 | 8.73 | 0.492 | -20.64 | -13.38 |
| Wt.Ave. | 1.38 | 0.580 | 1.20 | 0.38 | 11.00 | 0.568 | -- | -- |
| B-2. Intermediate Gettering (with $SiO_2$ glass on surface) | | | | | | | | |
| High | 1.43 | 0.575 | 1.26 | 0.44 | 13.40 | 0.680 | 8.94 | 5.43 |
| Low | 1.38 | 0.555 | 1.20 | 0.37 | 10.71 | 0.580 | -12.93 | -10.08 |
| Wt.Ave. | 1.40 | 0.565 | 1.24 | 0.41 | 12.30 | 0.645 | -- | -- |
| B-3. Pre-Gettering (with $SiO_2$ glass on surface) | | | | | | | | |
| High | 1.42 | 0.575 | 1.25 | 0.420 | 12.68 | 0.643 | 8.10 | 4.72 |
| Low | 1.37 | 0.560 | 1.10 | 0.370 | 9.83 | 0.531 | -16.20 | -13.52 |
| Wt.Ave. | 1.40 | 0.565 | 1.20 | 0.405 | 11.73 | 0.614 | -- | -- |
| B-4. Intermediate Gettering with SiO AR Coating | | | | | | | | |
| High | 1.46 | 0.573 | 1.30 | 0.455 | 14.29 | 0.712 | 7.61 | 3.79 |
| Low | 1.40 | 0.555 | 1.20 | 0.43 | 12.46 | 0.664 | -6.17 | -3.21 |
| Wt.Ave. | 1.43 | 0.565 | 1.28 | 0.43 | 13.28 | 0.686 | -- | -- |

The effect of SiO anti-reflective coating in conjunction with intermediate gettering is shown in Figure 16 and in Table 4. Batch B-4 has the highest average efficiency and the smallest efficiency and fill factor dispersions of all four batches. Batch B-5 solar cells with SiO A.R. coating had an increase in average efficiency of 8.0 percent over Batch B-2 solar cells without an A.R. coating, but with an $SiO_2$ glass surface and had an increase in average efficiency of 20.7 percent over the control batch B-1 solar cells, which were texturized without gettering but with an $SiO_2$ glass surface. The highest efficiency obtained was 14.29 percent. The average solar cell efficiency for Batch B-4 was 13.28 percent.

From the preceeding discussion, it is clear that low temperature intermediate gettering in conjunction with an A.R.coating will lead to higher average solar cell efficiency and smaller efficiency and fill factor dispersion than ungettered or pregettered solar cells. A large improvement in average solar cell efficiency can be achieved using low temperature intermediate gettering for fair quality silicon.

(e) Gettering Temperature Effects "Series C"

Experiments were performed to study the effect of gettering temperature on solar cell electrical performance. Three batches, which are designated "Series C", each consisting of thirty 3 inch (76mm) diameter silicon wafers were processed with the same Sensor Technology process given in Task 4(a) and with an intermediate gettering step for 35 minutes.

Electrical performance data for Batch C-1 through C-3 were determined from the corresponding I-V curves presented in Figures 17 through 19 respectively, and are summarized in Table 5. The batches are differentiated on the basis of the gettering temperature.

Batch C-1 was gettered at 1050°C. From Figure 17, it is clear that Batch C-1 has very large efficiency and fill factor dispersions. The electrical performance of many solar cells were severely impaired at this gettering temperature.

Batch C-2 was gettered at 975°C. Figure 18 clearly shows that Batch C-2 has a very large efficiency and fill factor dispersions. However, the average efficiency of Batch C-2 is higher than Batch C-1.

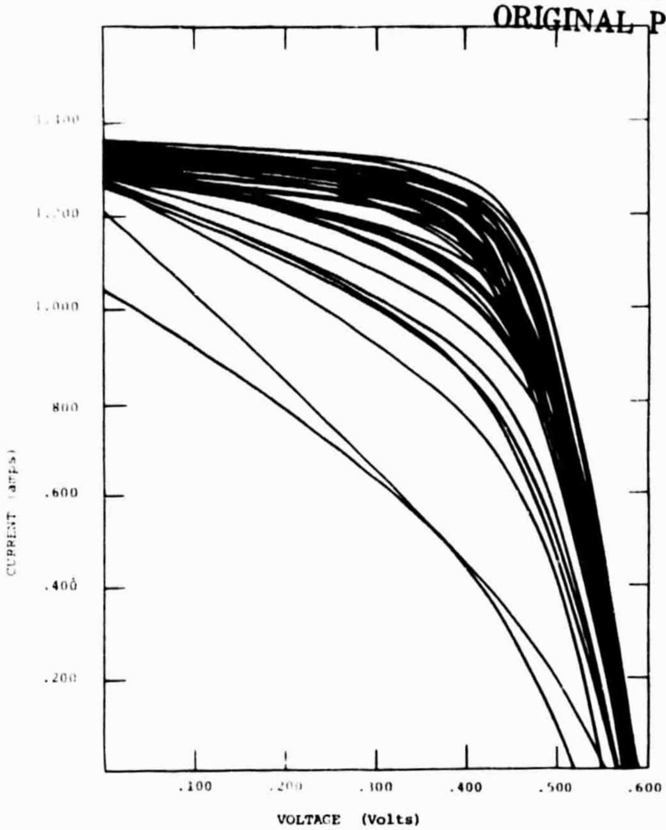


Figure 17: Electrical performance curves for 3 inch diameter intermediate gettered ($POCl_3$, 1050°C) solar cells, Batch C-1.

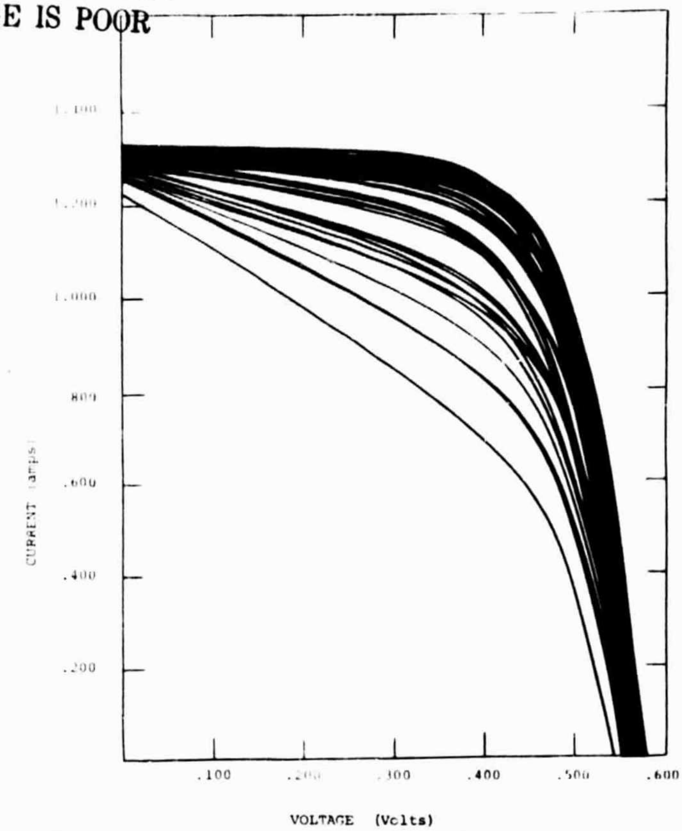


Figure 18: Electrical performance curves for 3 inch diameter intermediate gettered ($POCl_3$, 975°C) solar cells, Batch C-2.

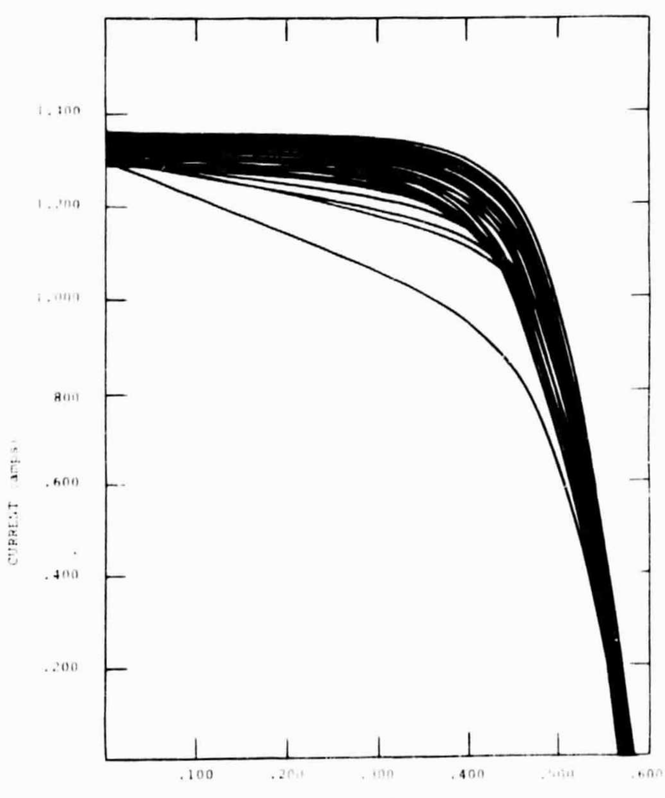


Figure 19: Electrical performance curves for 3 inch diameter intermediate gettered ($POCl_3$, 900°C) solar cells, Batch C-3.

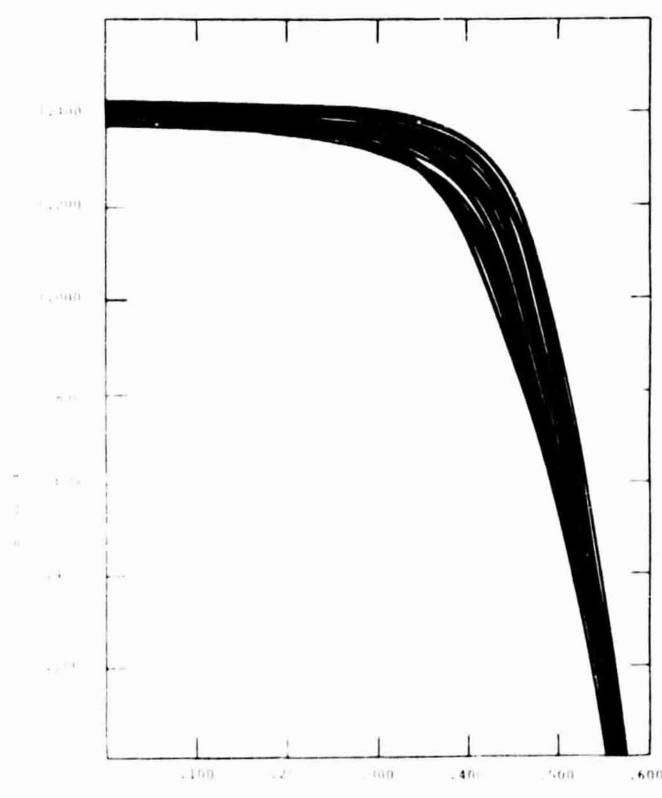


Figure 14: Electrical performance curves for 3 inch diameter intermediate gettered ($POCl_3$, 875°C) solar cells, Batch B-2.

Table 5. Solar cell electrical performance results on the effects of intermediate gettering temperature on fair quality 3 inch round silicon material.

| Batch | Isc (a) | Voc (v) | Ipp (a) | Vpp (v) | $\eta$ (%) | FF | $\frac{\Delta\eta}{\eta}$ (%) | $\frac{\Delta FF}{FF}$ (%) |
|---|---|---|---|---|---|---|---|---|
| C-1. Intermediate Gettering 1050°C, 35 min , Std. Two Step Tex., Std $POCl_3$ Diff. Std. Electroless Nickel Plating, Al Back, Solder, no A.R. Coating. | | | | | | | | |
| High | 1.36 | .585 | 1.22 | .435 | 12.80 | .667 | 18.63 | 12.27 |
| Low | 1.02 | .520 | .50 | .380 | 4.60 | .358 | -56.02 | -38.28 |
| Wt.Ave. | 1.30 | .575 | 1.02 | .425 | 10.46 | .580 | -- | -- |
| C-2. Intermediate Gettering (975°C, 35 min) | | | | | | | | |
| High | 1.32 | .580 | 1.17 | .45 | 12.70 | .688 | 14.41 | 9.03 |
| Low | 1.22 | .545 | .63 | .43 | 6.54 | .407 | -41.88 | -35.50 |
| Wt.Ave. | 1.29 | .565 | 1.07 | .43 | 11.10 | .631 | -- | -- |
| C-3. Intermediate Gettering (900°C, 35 min) | | | | | | | | |
| High | 1.34 | .585 | 1.23 | .44 | 13.06 | .690 | 7.58 | 3.29 |
| Low | 1.29 | .570 | 1.03 | .43 | 10.68 | .602 | -12.03 | -9.88 |
| Wt.Ave. | 1.31 | .575 | 1.17 | .43 | 12.14 | .668 | -- | -- |
| B-2. Intermediate Gettering (875°C, 35 min) | | | | | | | | |
| High | 1.43 | 0.575 | 1.26 | 0.44 | 13.40 | 0.680 | 8.94 | 5.43 |
| Low | 1.38 | 0.555 | 1.20 | 0.37 | 10.71 | 0.580 | -12.93 | -10.08 |
| Wt.Ave. | 1.40 | 0.565 | 1.24 | 0.4[illegible] | 12.30 | 0.645 | -- | -- |

Batch C-3 was gettered at 900°C and is characterized in Figure 19 by a well defined set of I-V curves. However, one I-V curve was low and was not included in the analysis shown in Table 5. Batch C-3 has a significantly higher average efficiency and small efficiency and fill factor dispersions than Batch C-1 or C-2.

Batch B-2, Figure 14, was gettered at 875°C and is included in Table 5 for comparison with Batches C-1, C-2 and C-3. Figure 14 shows a very well defined set of I-V curves with no low I-V curves found in this batch of solar cells. Furthermore, no I-V curves were found to be low in Batches P-4 (Figure 5), A-4 (Figure 10), and A-5 (Figure 11). The results, therefore, show that 875°C is the optimum intermediate gettering temperature within the temperature range studied in this task.

(f) Low-Cost Recycled Gettering "Series D"

Experiments were performed to investigate the practicality of recycling exhaust diffusion gasses to reduce the cost of the gettering step. The experimental set-up for this task is shown in Figure 20.

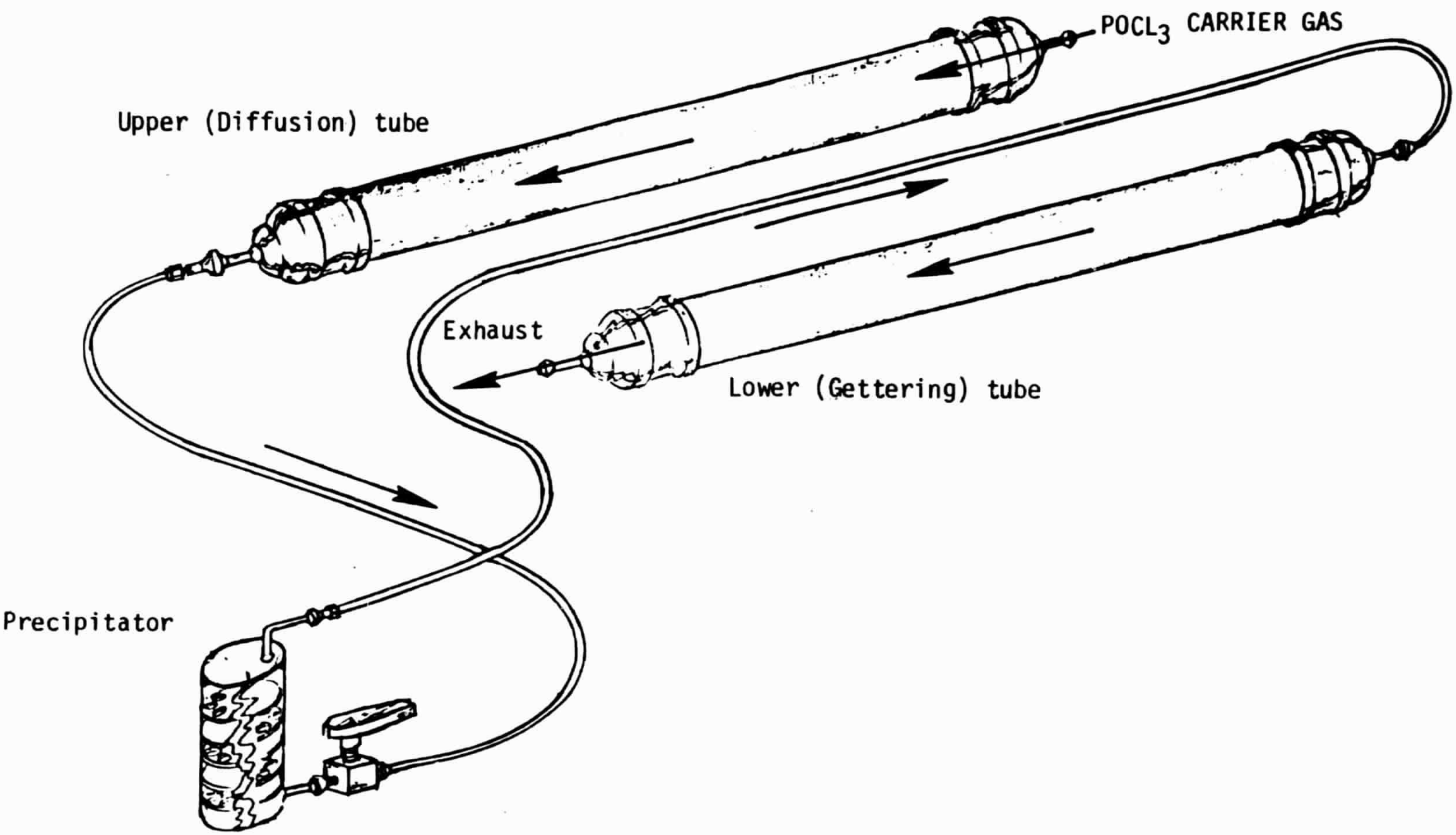


Figure 20: Equipmental set-up of the exhuast diffusion gas recycling system for the gettering process.

The mode of operation of this recycling system consists of the transport of exhaust diffusion gasses from the upper diffusion tube to the lower diffusion tube, via Teflon Tubing. Prior to entering the lower diffusion tube, the exhaust diffusion gasses are passed through a precipitator where particulates such as $P_2O_5$ are filtered out. Consequently, the gasses entering the diffusion tube are contamination free, and capable of generating phosphosilicate glass on the wafer surface. The recycling system described above will allow the diffusion to be performed in conjunction with the gettering process, i.e., diffusion occurs in the upper tube, and gettering occurs in the lower tube.

A total of three batch tests, designated as "Series D" were performed. All processing parameters were identical in each case with the exception of gettering temperature. The basic processing sequence utilized in each batch test is as follows:

(1) isotropic surface etch in HF solution (3 minutes).

(2) getter for 35 minutes with recycled $POCl_3$.

(3) isotropic surface etch in HF solution (1.5 minutes).

(4) $POCl_3$ diffusion, 45 min, 875°C).

(5) remaining steps are standard solar cell fabrication processes, with no A.R.coating.

The solar cells utilized in the recycling experiments had an active area of 42.6 $cm^2$. Batch D-1 was gettered at 1000°C. Batch D-2 was gettered at 925°C. Batch D-3 was gettered at 875°C. The I-V curves for Batches D-1, D-2 and D-3 are presented in Figure 21, 22 and 23 respectively. The I-V curves for each batch were analyzed and, relevant electrical performance characteristics are shown in Table 6.

The results indicated that gettering with recycled $POCl_3$ at 925°C in conjunction with isotropic surface etching in HF yields the narrowest efficiency dispersion. However, gettering with recycled $POCl_3$ at 875°C in conjunction with isotropic surface etching in HF produced solar cells with the highest average efficiency 10.4% for the solar cells processed in this task.

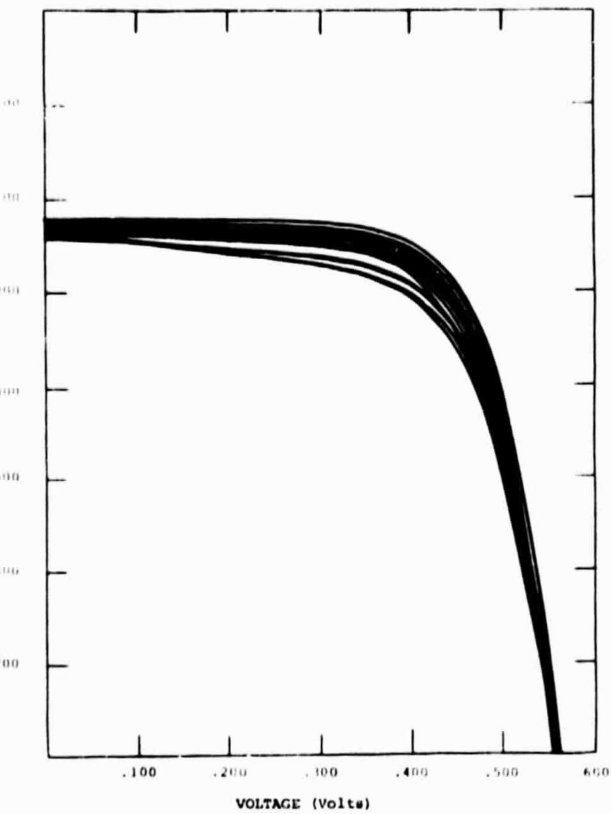


Figure 21: Electrical performance curves for Batch D-1 solar cells which were surface etched and intermediate gettered at 1000°C with recycled $POCl_3$.

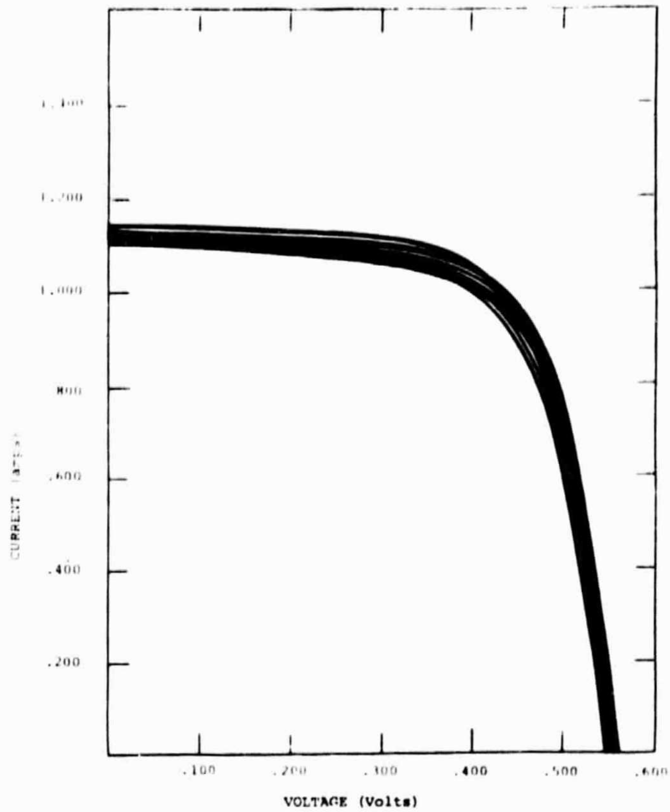


Figure 22: Electrical performance curves for Batch D-2 solar cells which were surface etched and intermediate gettered at 925°C with recycled $POCl_3$.

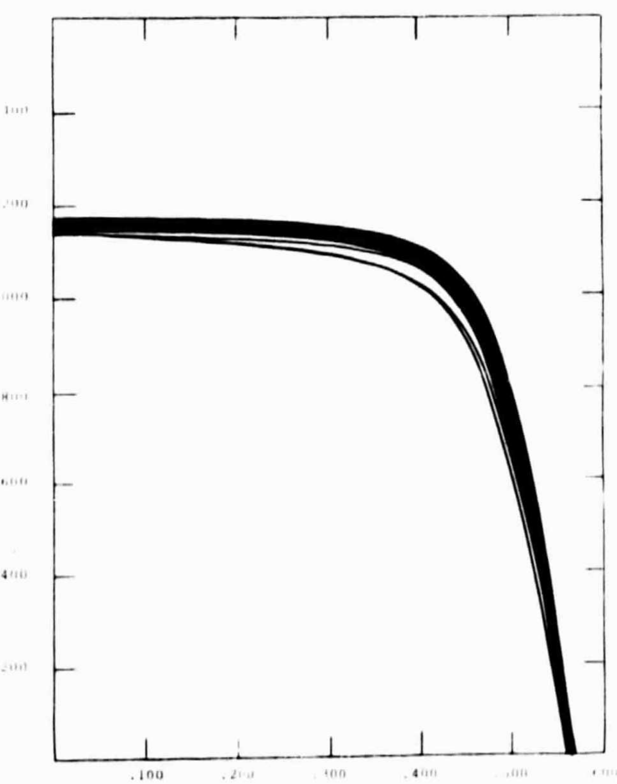


Figure 23: Electrical performance curves for Batch D-3 solar cells which were surface etched and intermediate gettered at 875°C with recycled $POCl_3$.

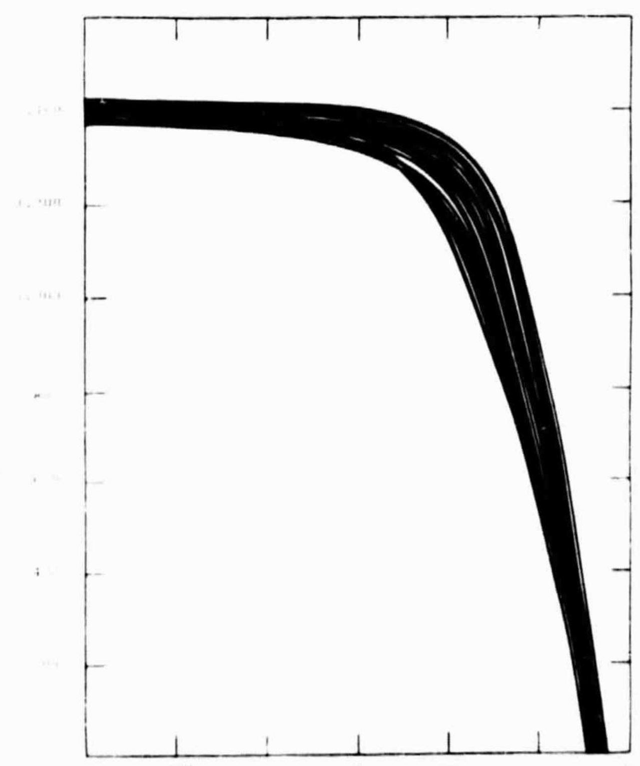


Figure 24: Electrical performance curves for 3 inch diameter intermediate gettered ($POCl_3$, 875°C) solar cells, Batch B-2.

Table 6. Solar cell electrical performance results showing the effects of recycled intermediate gettering at various temperatures on fair quality 3 inch diameter surface etched silicon material.

| Batch | Isc (a) | Voc (v) | Ipp (a) | Vpp (v) | η (%) | FF | $\frac{\Delta\eta(\%)}{\eta}$ | $\frac{\Delta FF(\%)}{FF}$ |
|---|---|---|---|---|---|---|---|---|
| D-1 Intermediate gettered at 1000°C (recycled). | | | | | | | | |
| High | 1.16 | .560 | 1.03 | .445 | 10.76 | .710 | 5.74 | 2.90 |
| Low | 1.11 | .550 | .94 | .43 | 9.48 | .662 | -6.79 | -4.06 |
| Wt.Ave. | 1.14 | .555 | 1.02 | .425 | 10.18 | .690 | | |
| D-2 Intermediate gettered at 925°C (recycled). | | | | | | | | |
| High | 1.14 | .565 | .98 | .455 | 10.47 | .690 | 4.36 | 2.22 |
| Low | 1.11 | .555 | .92 | .440 | 9.50 | .657 | -5.24 | -2.67 |
| Wt.Ave. | 1.13 | .560 | .96 | .445 | 10.03 | .675 | | |
| D-3 Intermediate gettered at 875°C (recycled). | | | | | | | | |
| High | 1.16 | .565 | 1.03 | .450 | 10.88 | .710 | 4.29 | 2.90 |
| Low | 1.13 | .555 | .95 | .430 | 9.59 | .650 | -8.02 | -5.80 |
| Wt.Ave. | 1.15 | .560 | 1.01 | .440 | 10.43 | .690 | | |
| B-2 Intermediate gettering with texturizing. | | | | | | | | |
| High | 1.43 | .575 | 1.26 | .44 | 13.40 | .680 | 8.94 | 5.43 |
| Low | 1.38 | .555 | 1.20 | .37 | 10.71 | .580 | -12.93 | -10.08 |
| Wt.Ave. | 1.40 | .565 | 1.24 | .41 | 12.30 | .645 | | |

Batch B-2, Figure 14, was texturized and intermediate gettered at 875°C and is included in Table 6 for comparison with the surface etched and intermediate gettered Batch D-3 solar cells. Both batches of solar cells are characterized by a well defined set of I-V curves. The average efficiency, 12.3%, of the texturized gettered batch of solar cells was found to be 18.3 percent higher than the average efficiency, 10.4%, of the isotropic surface etched/gettered solar cells. This efficiency improvement achieves one of the specific goals for this wafer surface texturizing study of the near term implementation of flat plate photovoltaic cost reduction.

(g) <u>Summary of Texturizing/Gettering Results</u>

A summary of texturizing/gettering batch test results for fair quality silicon wafer material is given in Table 7. Included in the table are the preliminary electrical performance results, "Series P", with gettering placement and temperature; texturizing/gettering and A.R.coating effects, "Series B", on fair quality silicon wafer material ($POCl_3$ gettering temperature was held at 875°C for 35 minutes); intermediate gettering temperature effects, "Series C" on fair quality silicon wafer material; and recycled

gettering effect, "Series D", on isotropic surface etched wafers. A detailed discussion of the general trends and conclusions is presented in a separate section of this report.

A summary of the texturizing/gettering/ spray-on doped batch test results "Series A", for low quality silicon wafer material is given in Table 8. Included in the table is effects of texturizing, $SiO_2$ glass removal, gettering placement, and A.R. coating on spray-on $n^+$ and $p^+$ doped solar cells. A comparison of $POCl_3$ diffused solar cells and spray-on doped solar cells is also given in the table. A discussion of the general trends is presented in the conclusion section of this report.

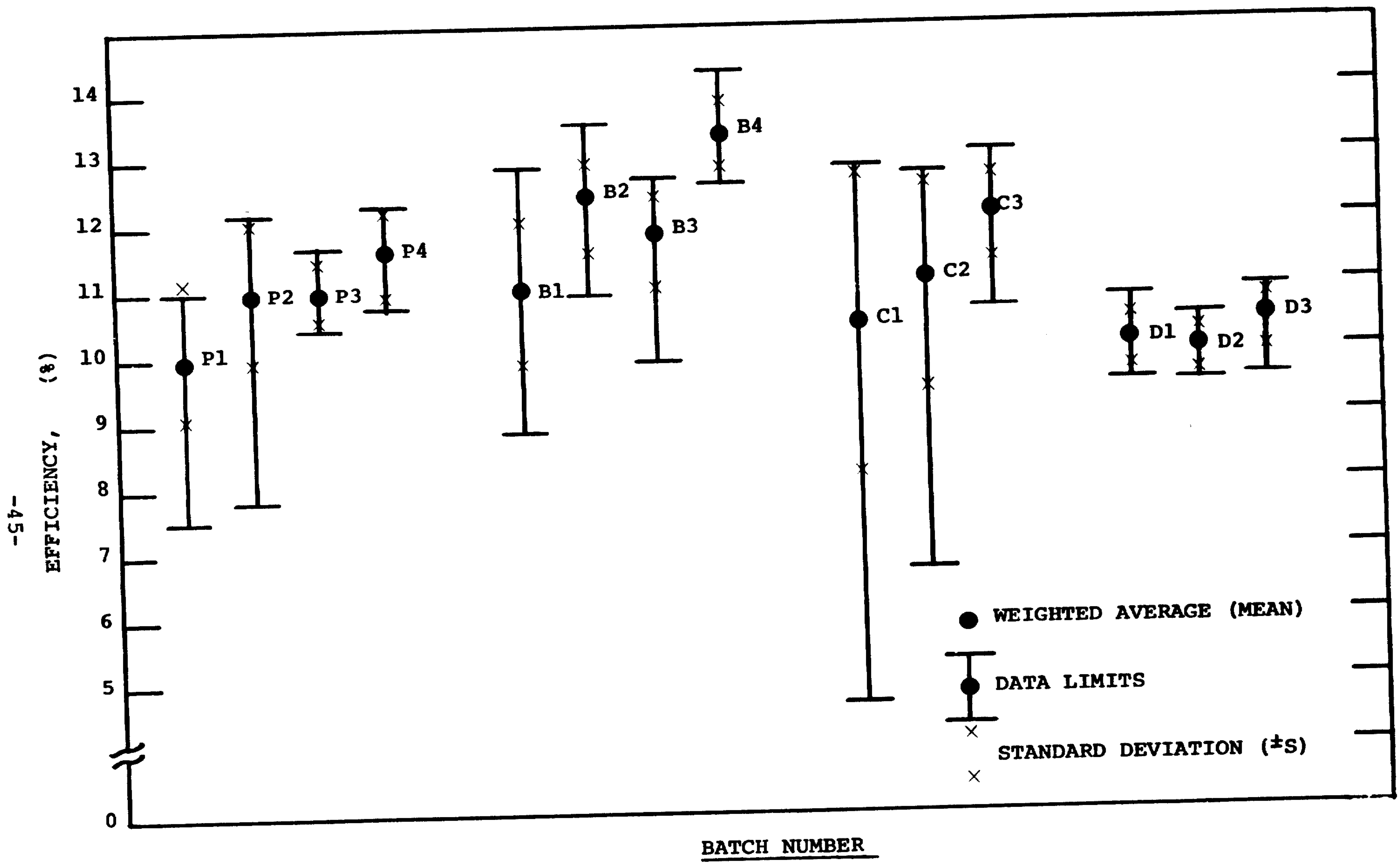


Table 7. Summary of texturizing/gettering batch test results for fair quality silicon wafer material.

## TEXTURIZING/GETTERING BATCH TESTS

P 1 - Control Cells, Texturized, 54.91cm$^2$ Active Area

P 2 - Intermediate Gettered (1000$^{\circ}$C)

P 3 - Pregettered (875$^{\circ}$C)

P 4 - Intermediate Gettered (875$^{\circ}$C)

B 1 - Control Cells, Texturized, 41.4cm$^2$ Active Area

B 2 - Intermediate Gettered (875$^{\circ}$C)

B 3 - Pregettered (875$^{\circ}$C)

B 4 - Intermediate Gettered (875$^{\circ}$C) With SiO

C 1 - Intermediate Gettered (1050$^{\circ}$C), 41.4cm$^2$ Active Area

C 2 - Intermediate Gettered (975$^{\circ}$C)

C 3 - Intermediate Gettered (900$^{\circ}$C)

D 1 - Control Cells, Surface Etched, 42.6cm$^2$ Active Area & Intermediate Gettered (1000$^{\circ}$C)

D 2 - Intermediate Gettered (925$^{\circ}$C)

D 3 - Intermediate Gettered (875$^{\circ}$C)

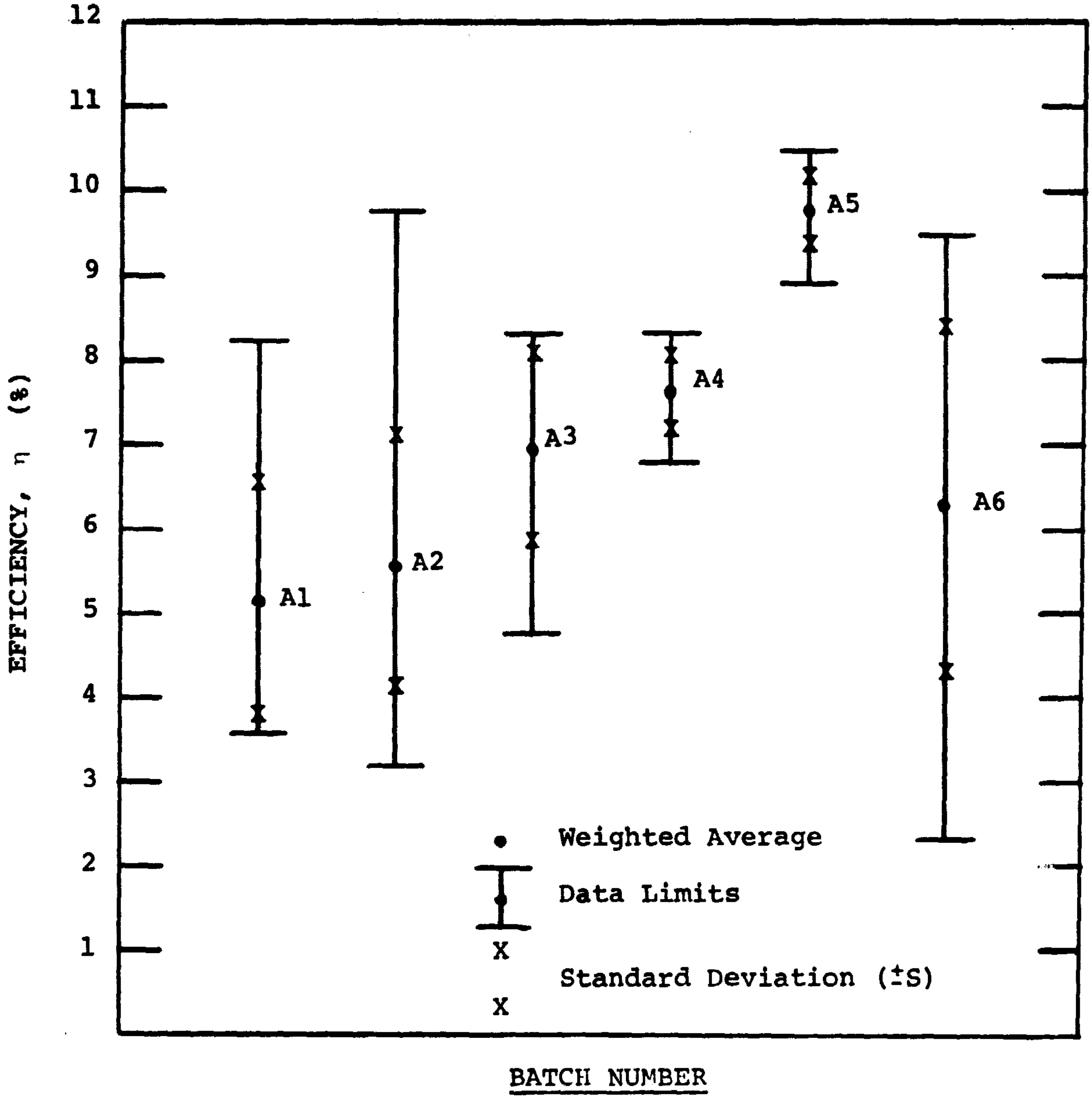


Table 8. Summary of texturizing/gettering/spray-on dopant batch tests results for low quality silicon wafer material.

## TEXTURIZING/GETTERING/
## SPRAY-ON DOPANT BATCH TESTS

A 1 - Control Cells, Spray-on Doped ($n^+$ and $p^+$), Texturized, $12.75 cm^2$ Active Area, Nonoptimized Grid Pattern. Cells Cut Square by Laserscribe From 2.15 Inch Diameter Solar Cells.

A 2 - $SiO_2$ Glass Removed

A 3 - Pregettered ($875^oC$)

A 4 - Intermediate Gettered ($875^oC$)

A 5 - Intermediate Gettered ($875^oC$) with SiO

A 6 - Texturized, $POCl_3$ Diffused with SiO

## PROCESS/EQUIPMENT COST ANALYSIS

A cost analysis was performed using the Solar Array Manufacturing Industry Costing Standards (SAMICS) on the four process steps investigated under this program. A standard Format A was prepared according to JPL Document Number 5101-44 Revision A[10] and JPL Document Number 5101-59 [11] for the four process tasks listed below:

(1) Low-Cost Wafer Cleaning

(2) Two-Stage Texturizing Process

(3) Low-Cost Wafer Drying

(4) Gettering Process

The process costs for each step were computed manually according to the SAMICS Workbook, JPL Document 5101-15[12]. The unit prices for the direct material cost elements were obtained from the Cost Account Catalog of the SAMIS II computer program [13].

The basic assumptions used to compute the added cost of each process step are as follows:

(1) 1986 standard industry, 500$MW_{pk}$ per year.

(2) Production volume will be 200$MW_{pk}$ per year or 40% of the total market.

(3) Cell efficiency after encapsulation is 13%; cell size is 3 inch diameter with an effective area of 7.087 $in^2$ (45.6 $cm^2$); peak power per cell is 0.593 watts.

(4) Number of cells produced per year is 338 million.

(5) Initial wafer cost was set equal to zero. This will allow one to obtain the cost due exclusively to the process; the process yield was set equal to 100 percent.

The cost for each process step was computed separately and the results are presented in Table 7. The results show that the total texturizing cost amounts to 1.26 cents per peak watt and the cost added by the gettering step is 0.97 cents per peak watt. In view of the JPL/LSA 1986 price goal of 50 cents per peak watt (in 1975 cents) the wafer surface preparation cost, including the texturization and gettering process steps, is an acceptable cost. The added cost of the recycled gettering step (2% of the total cell process cost) is more than justified because at least a 10 percent gain in average cell efficiency can be achieved with the inclusion of this process step.

Table 9. Summary of Wafer Surface Preparation Costs For 1986 in 1975 Cents Per Peak Watt.

| COST ELEMENTS | WAFER CLEANING* | TWO STAGE TEXTURIZING | HOT AIR DRYING | SUBTOTAL | RECYCLE GETTERING* | TOTAL |
|---|---|---|---|---|---|---|
| Equipment | 0.023 | 0.079 | 0.035 | 0.137 | 0.316 | 0.453 |
| Floorspace | 0.017 | 0.013 | 0.020 | 0.050 | 0.098 | 0.148 |
| Labor | 0.563 | 0.164 | 0.117 | 0.844 | 0.477 | 1.321 |
| Material | 0.057 | 0.004 | 0.114 | 0.175 | -0- | 0.175 |
| Utilities | 0.024 | 0.022 | 0.006 | 0.052 | 0.077 | 0.129 |
| TOTAL | 0.684 | 0.282 | 0.292 | 1.258 | 0.968 | 2.223 |

* Used currently available machines.

## CONCLUSIONS

The work performed in the silicon wafer surface texturizing program led to a number of conclusions which are listed by task below:

### LOW-COST WAFER CLEANING

(1) A low-cost silicon wafer cleaning method was found to be suitable for large scale production.

(2) The cleaning method used recycled Freon TMS in an ultrasonic vapor degreaser.

(3) The cost goal was achieved. The cost for silicon wafer cleaning was found to be less than 0.7 cents per peak watt.

### LOW-COST WAFER DRYING

(1) A low-cost clean dry air system was found to be suitable for large scale production.

(2) A low-cost clean dry air system can replace a high cost dry nitrogen system without any adverse effects on solar cell electrical performance. The clean air unit acquired in this project effectively removed the moisture

content of the air and eliminated oil and dust particles.

(3) Air convection drying was shown not to be cost effective due to the long drying time required.

(4) A forced air dry tunnel system was found to be cost effective at an initial wafer drying temperature of 80°C. The technique is suitable for surface etched and texturized silicon wafers.

TWO STAGE TEXTURIZING PROCESS

(1) Under laboratory conditions, where the initial wafer surface characteristics, i.e. surface contaminants, saw marks and chips, are controlled, the processing time for each step in the two-stage texturizing process (10%/1% NaOH) is five minutes.

(2) In large scale production, where currently the wafer surface characteristics are not controlled, the processing time was found to be variable and require more than five minutes. These wafers are typically received from more than one supplier and have severely contaminated and damaged surfaces.

## GETTERING PROCESS

(1) A large improvement in average solar cell efficiency can be achieved by utilizing a low temperature gettering treatment in combination with a two stage texturizing process sequence.

(2) Intermediate gettering produced the highest average solar cell batch efficiency, 13.3% (with SiO) in production. Intermediate gettering with $POCl_3$ is performed between the two NaOH etching solutions in the two stage texturizing process.

(3) The highest solar cell efficiency achieved in production was 14.3%.

(4) The optimum intermediate gettering temperature and time was found to be 875°C for 35 minutes, for the range of temperatures examined in this program.

(5) Low temperature intermediate gettering minimized efficiency and fill factor dispersions.

(6) Gettering improved the quality of silicon wafer batch material. Quality of silicon material was defined in terms of the characteristic I-V curves for a batch of solar cells.

(7) The gettering effect was more pronounced on low quality silicon wafer material than on fair quality silicon wafer material.

(8) The electrical performance of texturized, spray-on doped solar cells is very similar to the electrical performance of texturized, $POCl_3$ diffused solar cells.

(9) Low temperature gettering improved the electrical performance of spray-on doped solar cells.

(10) Low temperature gettered, spray-on doped solar cells had significantly higher average efficiency, and smaller efficiency and fill factor dispersion than ungettered, $POCl_3$ diffused solar cells.

(11) Low temperature intermediate gettering with the $SiO_2$ glass removed and an A.R. coating (SiO) applied led to a higher average solar cell efficiency and lower efficiency and fill factor dispersion than ungettered or pregettered solar cells.

(12) An 8.0% average batch efficiency improvement was observed with intermediate gettered and SiO A.R.coated solar cells over intermediate gettered solar cells with $SiO_2$ glass.

(13) An 11.8% average batch efficiency improvement was observed for intermediate gettered solar cells over texturized (no gettering) solar cells.

(14) Recycled gettering was found to be feasible and cost effective.

(15) The average production efficiency 12.3% (without an A.R.coating) of the texturized/gettered batch of solar cells was found to be 18.3% higher than the average efficiency, 10.4% of the isotropic surface etched/gettered batch of solar cells.

(16) The efficiency goal was achieved for the wafer surface texturizing study for the near term implementation of flat plate photovoltaic cost reduction.

PROCESS/EQUIPMENT COST ANALYSIS

(1) The texturizing process cost including cleaning, drying, and texturizing amounted to 1.26 cents per peak watt (1975 cents).

(2) The recycled gettering cost was found to be 0.97 cents per peak watt.

(3) The wafer surface preparation cost including the texturizing process and gettering process steps was found to be in line with the 1986 DOE/JPL Low-Cost Solar Array project goal (in 1975 cents) of 50 cents per peak watt.

## RECOMMENDATIONS

In large scale production, where currently the wafer surface characteristics are not controlled, the processing time was found to be variable and to require more than five minutes for each etching step. These wafers are typically received from more than one supplier and may have surfaces which are severely contaminated and damaged. An optimum etching time for a given characteristic batch of silicon wafers was beyond the scope of this program. It is recommended that an analysis of as-cut silicon wafer surface characteristics versus etching time be made in large scale production.

The texturizing/gettering data in this program was examined primarily to determine general trends and process characteristics which are applicable for near term implementation in large scale production. An in-depth qualitative analysis for cause and effect was not performed in this program. It is recommended that for example, SEM surface analysis of the texturized/gettered surface be made, bulk and surface resistivity be measured, lifetime measurements be made, and solar cell spectral response be investigated for solar cells fabricated using the texturizing/gettering process steps.

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